



A7682S R5

Hardware Design

LTE Module

SIMCom Wireless Solutions Limited

SIMCom Headquarters Building, Building 3, No. 289 Linhong
Road, Changning District, Shanghai P.R. China

Tel: 86-21-31575100

support@simcom.com

www.simcom.com

Document Title:	A7682S R5 Hardware Design
Version:	V1.00
Date:	2024-03-13
Status:	Draft

GENERAL NOTES

SIMCOM OFFERS THIS INFORMATION AS A SERVICE TO ITS CUSTOMERS, TO SUPPORT APPLICATION AND ENGINEERING EFFORTS THAT USE THE PRODUCTS DESIGNED BY SIMCOM. THE INFORMATION PROVIDED IS BASED UPON REQUIREMENTS SPECIFICALLY PROVIDED TO SIMCOM BY THE CUSTOMERS. SIMCOM HAS NOT UNDERTAKEN ANY INDEPENDENT SEARCH FOR ADDITIONAL RELEVANT INFORMATION, INCLUDING ANY INFORMATION THAT MAY BE IN THE CUSTOMER'S POSSESSION. FURTHERMORE, SYSTEM VALIDATION OF THIS PRODUCT DESIGNED BY SIMCOM WITHIN A LARGER ELECTRONIC SYSTEM REMAINS THE RESPONSIBILITY OF THE CUSTOMER OR THE CUSTOMER'S SYSTEM INTEGRATOR. ALL SPECIFICATIONS SUPPLIED HEREIN ARE SUBJECT TO CHANGE.

COPYRIGHT

THIS DOCUMENT CONTAINS PROPRIETARY TECHNICAL INFORMATION WHICH IS THE PROPERTY OF SIMCOM WIRELESS SOLUTIONS LIMITED. COPYING, TO OTHERS AND USING THIS DOCUMENT, ARE FORBIDDEN WITHOUT EXPRESS AUTHORITY BY SIMCOM. OFFENDERS ARE LIABLE TO THE PAYMENT OF INDEMNIFICATIONS. ALL RIGHTS RESERVED BY SIMCOM IN THE PROPRIETARY TECHNICAL INFORMATION, INCLUDING BUT NOT LIMITED TO REGISTRATION GRANTING OF A PATENT, A UTILITY MODEL OR DESIGN. ALL SPECIFICATION SUPPLIED HEREIN ARE SUBJECT TO CHANGE WITHOUT NOTICE AT ANY TIME.

SIMCom Wireless Solutions Limited

SIMCom Headquarters Building, Building 3, No. 289 Linhong Road, Changning District, Shanghai P.R. China

Tel: +86 21 31575100

Email: simcom@simcom.com

For more information, please visit:

<https://www.simcom.com/download/list-863-en.html>

For technical support, or to report documentation errors, please visit:

<https://www.simcom.com/ask/> or email to: support@simcom.com

Copyright © 2024 SIMCom Wireless Solutions Limited All Rights Reserved.

Version History

Date	Version	Description of change	Author
2024-03-13	1.00	Initial	Han.Gao

SIMCom
Confidential

Contents

1. Introduction	9
1.1. Documentation Overview	9
1.2. Product Outline	10
1.3. Hardware Interface Overview	11
1.4. Hardware Block Diagram	12
1.5. Functional Overview	12
2. Package Information	14
2.1. Pin Assignment Overview	14
2.2. Pin Description	16
2.3. Mechanical Information	22
3. Interface Application	23
3.1. Power Supply	23
3.1.1. Power Supply Design Guide	24
3.1.2. Recommended Power Supply Circuit	25
3.1.3. Voltage Monitor	26
3.2. Power On/ Off and Reset	27
3.2.1. Power on	27
3.2.2. Power off	28
3.2.3. Reset Function	30
3.3. UART Interface	31
3.3.1. UART Design Guide	32
3.3.2. RI and DTR Behavior	34
3.3.3. DTR Function Description	34
3.4. USB Interface	35
3.4.1. USB Reference Design	35
3.4.2. USB_BOOT Interface	36
3.5. USIM Interface	38
3.5.1. SIM Hot Swap Function	39
3.5.2. SIM Application Guide	40
3.6. SPI Interface	41
3.7. Audio Interface	42
3.7.1. Analog Audio Onput Interface	42
3.7.2. Analog Audio Reference Design	42
3.8. I2C Interface	43
3.9. LCD Interface	44
3.10. GPIO Interface	45
3.11. STATUS Interface	46
3.12. NETLIGHT Interface	47
3.13. Other Interface	48
3.13.1. ADC	48
3.13.2. VDD_EXT	49

4. RF Specifications	51
4.1. LTE Specifications	51
4.2. LTE Antenna Requirements	52
4.3. Antenna Reference Design	53
4.3.1. Passive Antenna for LTE/GNSS	53
4.3.2. Active Antenna for GNSS	54
4.4. PCB layout	55
5. Electrical Specifications	56
5.1. Absolute maximum ratings	56
5.2. Operating conditions	56
5.3. Operating Mode	57
5.3.1. Operating Mode Definition	57
5.3.2. Sleep mode	58
5.3.3. Minimum functionality mode and Flight mode	59
5.3.4. PSM mode	60
5.4. Current Consumption	60
5.4.1. Current Consumption of VBAT	60
5.4.2. Current Consumption of GNSS	61
5.5. ESD Notes	61
6. SMT Production Guide	63
6.1. Top and Bottom View of the module	63
6.2. Label Information	64
6.3. Recommended PCB Footprint	65
6.4. Recommended SMT Stencil	66
6.5. Recommended reflow furnace temperature curve	67
6.6. Moisture Sensitivity Level (MSL)	68
6.7. Baking Requirements	70
7. Packaging	71
8. Appendix	74
8.1. Coding Schemes and Maximum Net Data Rates over Air Interface	74
8.2. Related Documents	74
8.3. Terms and Abbreviations	76
8.4. Safety Caution	78

Table Index

Table 1: A7682S R5 Series Documents Overview	9
Table 2: Module frequency bands.....	10
Table 3: Module feature difference	10
Table 4: General features	12
Table 5: Pin Description	15
Table 6: Pin parameter abbreviation.....	16
Table 7: 1.8V IO parameters definition	16
Table 8: 3.0V IO parameters definition	17
Table 9: Pin description.....	18
Table 10: Power interface pins definition.....	23
Table 11: VBAT pins electronic characteristic.....	23
Table 12: TVS for VBAT part number list.....	25
Table 13: PWRKEY interface pin definition	27
Table 14: Power on timing and electronic characteristic	28
Table 15: Power off sequence parameters.....	29
Table 16: RESET interface pin definition	30
Table 17: RESET pin electronic characteristic	31
Table 18: UART information.....	31
Table 19: UART interface pins definition	31
Table 20: USB interface pins definition.....	35
Table 21: TVS for USB part number list.....	36
Table 22: USB_BOOT interface pin definition	37
Table 23: USIM interface pins definition	38
Table 24: USIM electronic characteristic in 1.8V mode (SIM_VDD=1.8V).....	39
Table 25: USIM electronic characteristic in 3.0V mode (SIM_VDD=3V).....	39
Table 26: TVS for USIM socket part number list	41
Table 27: SPI interface pins definition	41
Table 28: Analog audio output interface definition.....	42
Table 29: I2C interface pins definition.....	43
Table 30: LCD interface description.....	45
Table 31: Standard GPIO Resources of A7682S R5.....	45
Table 32: STATUS interface pin definition	46
Table 33: NETLIGHT interface pin definition	47
Table 34: LTE mode NETLIGHT pin status	48
Table 35: ADC interface pins definition.....	48
Table 36: General ADC electronic characteristics	48
Table 37: VDD_EXT interface pin definition	49
Table 38: VDD_EXT electrical characteristics	49
Table 39: TVS for VDD_EXT part number list	50
Table 40: Conducted transmission power	51
Table 41: E-UTRA operating bands	51

Table 42: Conducted receive sensitivity	51
Table 43: Reference sensitivity (QPSK)	52
Table 44: LTE antenna requirements.....	52
Table 45: TVS for RF main antenna part number list	53
Table 46: TVS for GNSS antenna part number list.....	54
Table 47: Absolute maximum ratings.....	56
Table 48: Recommended operating ratings.....	56
Table 49: 1.8V Digital I/O characteristics*	56
Table 50: Operating temperature	57
Table 51: Operating mode Definition	58
Table 52: Current consumption on VBAT Pins (VBAT=3.8V)	60
Table 53: Current consumption on VBAT Pins (VBAT=3.8V)	61
Table 54: The ESD performance measurement table (Temperature: 25℃, Humidity: 45%)	62
Table 55: The description of label information	64
Table 56: The main board reflux temperature curve requirements (lead-free)	67
Table 57: Moisture Sensitivity Level	69
Table 58: Module baking requirements	70
Table 59: Tray size	72
Table 60: Small Carton size	72
Table 61: Big Carton size	73
Table 62: Coding Schemes and Maximum Net Data Rates over Air Interface	74
Table 63: Related Documents	74
Table 64: Terms and Abbreviations.....	76
Table 65: Safety Caution.....	78

Figure Index

Figure 1: A7682S R5 block diagram.....	12
Figure 2: Pin assignment overview for A7682S R5.....	14
Figure 3: Dimensions (Unit: mm).....	22
Figure 4: Power supply application circuit.....	24
Figure 5: Power supply reference circuit.....	26
Figure 6: Power-off and power-on restart sequence.....	26
Figure 7: Reference power on/off circuit.....	27
Figure 8: Power on sequence.....	28
Figure 9: Power off timing sequence.....	29
Figure 10: Reference reset circuit.....	30
Figure 11: Serial port connection diagram (Full-function mode).....	32
Figure 12: Serial port connection diagram (NULL mode).....	33
Figure 13: Triode level conversion circuit.....	33
Figure 14: RI behaviour (SMS and URC report).....	34
Figure 15: USB circuit diagram.....	35
Figure 16: Reference USB_BOOT circuit.....	37
Figure 17: The USB port.....	38
Figure 18: SIM interface reference circuit.....	40
Figure 19: SIM interface reference circuit (8PIN).....	40
Figure 20: SPI reference circuit.....	42
Figure 21: Analog audio reference circuit.....	43
Figure 22: I2C reference circuit.....	44
Figure 23: STATUS reference circuit.....	46
Figure 24: NETLIGHT reference circuit.....	47
Figure 25: VDD_EXT reference circuit.....	49
Figure 26: Passive antenna reference.....	53
Figure 27: Active antenna reference.....	54
Figure 28: Reference PCB layout.....	55
Figure 29: Top and bottom view of the module.....	63
Figure 30: Label description of the module.....	64
Figure 31: Footprint recommendation (Unit: mm).....	65
Figure 32: Recommended SMT stencil (Unit: mm).....	66
Figure 33: Recommended reflow furnace temperature curve (lead-free).....	67
Figure 34: Humidity card.....	69
Figure 35: Packaging diagram.....	71
Figure 36: Tray drawing.....	71
Figure 37: Small carton drawing.....	72
Figure 38: Big carton drawing.....	72

1. Introduction

This document describes the electronic specifications, RF specifications, interfaces, mechanical characteristics, and test results of the A7682S R5 module. With the help of this document, customers can quickly understand the A7682S R5 module.

Referring to other software application notes and user guides, customers can use module to design and develop applications easily. SIMCom provides a set of evaluation boards to test easily and develop A7682S R5 module. The evaluation board tools include an EVB board, a USB cable, an antenna and other peripherals.

1.1. Documentation Overview

The documents listed in Table 1 primarily cover the module's technical information. To thoroughly understand the device and its application, it is necessary to study all relevant documents.

Table 1: A7682S R5 Series Documents Overview

No.	Document	Description
1	A7682S R5_Hardware_Design (This document)	Mainly introducing interface functions, recommend circuit, PCB layout guidelines, packaging and other hardware components, as well as the use of AT commands
2	SIMCom_A7680C series_Reference_Design_230809	Reference circuit applications
3	8BG000-A7680C-TE_V3.01_SCH&PCB	TE SCH&PCB PDF Document
4	SIMCOM_EVB_DL&PCB	SIMCOM_EVB SCH&PCB PDF Document
5	MOD_A7680C-R5_92(230607)	Reference Package (Pads)
6	A1602 & 1606_Series_AT_Command Manual	AT Command Manual
7	Module Secondary SMT Process User Guide	Module Secondary SMT Guidelines
8	SIMCOM EVB Kit User Guide	EVB Kit User Guide Document
9	A76XX_Series_CAT1_Module_Schematic&Layout_checklist	Peripheral circuit schematic and PCB checklist

NOTE

This current revision is an early release to support initial product developers. The content is subject to change without advance notice.

1.2. Product Outline

The module supports LTE-FDD and LTE-TDD. The supported radio frequency bands are described in the following table.

Table 2: Module frequency bands

Standard	Frequency	A7682S-LNXV	A7682S-MNXV
LTE-FDD	LTE-FDD B1	✓	✓
	LTE-FDD B3	✓	✓
	LTE-FDD B5	✓	✓
	LTE-FDD B8	✓	✓
LTE-TDD	LTE-TDD B34	✓	✓
	LTE-TDD B38	✓	✓
	LTE-TDD B39	✓	
	LTE-TDD B40	✓	✓
	LTE-TDD B41	✓	✓
Category	CAT1		

Table 3: Module feature difference

Function	A7682S-LNXV	A7682S-MNXV
GNSS		✓
USIM	✓	✓
Analog Audio Output	✓	✓
LCD	✓	✓
Wi-Fi Scan	✓	✓
FOTA	✓	✓
SMS	✓	

NOTE

The functions supported by the module are subject to the actual hardware model and software version.

With a small physical dimension of 15.7*17.6*2.1mm, the module can meet almost any space requirement in customers' applications, such as telematics, surveillance devices, industrial routers remote diagnostics, etc.

The module provides 92 pins, including 42 LCC pins in the outer ring and 50 LGA pins in the inner ring. This document will introduce all the functional pins.

1.3. Hardware Interface Overview

The interfaces are described in detail in the following chapters, including:

- Power supply
- USB 2.0 interface
- Three UART interfaces, only R5 LNXV supports two UART interfaces, one full function serial port, one ordinary serial port and one debug serial port. MNXV supports two UART interfaces.
- One USIM interface
- I2C interface
- ADC interface
- LCD interface
- General input and output interfaces (GPIOs)
- USB boot download and guidance interface
- One analog audio output interface
- Module operation status indication interface
- Network status indication interface
- Antenna interface

1.4. Hardware Block Diagram

The block diagram of the A7682S R5 module is shown in the figure below.

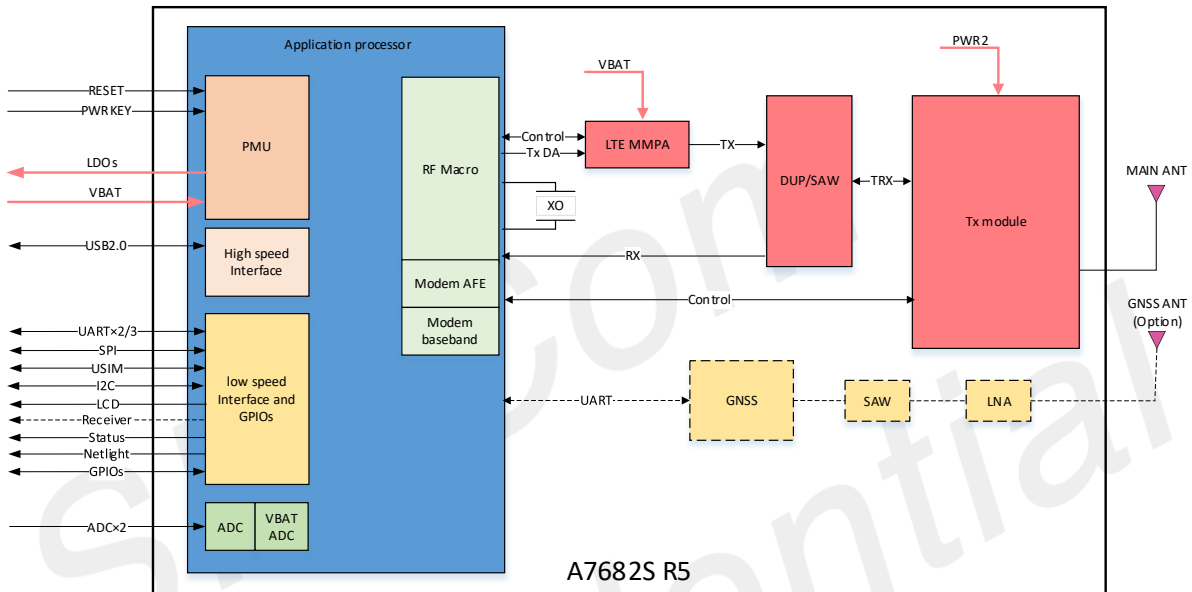


Figure 1: A7682S R5 block diagram

1.5. Functional Overview

Table 4: General features

Feature	Implementation
Power supply	VBAT: 3.4V~4.2V, Recommended VBAT: 3.8V
Power saving	Current in Sleep mode@DRX=0.32S typical: 1.22mA Current in Sleep mode@DRX=0.64S typical: 0.92mA Current in Sleep mode@DRX=1.28S typical: 0.7mA Current in Sleep mode@DRX=2.56S typical: 0.61mA Current in PSM mode typical: 8uA Please refer to the table 52
Radio frequency bands	Please refer to the table 2
Transmitting power	LTE power level: 3 (23dBm±2.7dB)
Data Transmission Throughput	TDD/FDD-LTE category 1 : 10 Mbps (DL), 5 Mbps (UL)
Antenna	LTE antenna interface GNSS antenna interface(optional)

SMS	• MT, MO, CB, Text, PDU mode • Short Message (SMS) storage device: USIM Card, CB does not support saving in SIM Card • Support CS and PS domain SMS
USIM interface	Support identity card: 1.8V/ 3V
USIM application toolkit	Support SAT class 3, GSM 11.14 Release 98 Support USAT
Phonebook management	Support phonebook types: SM/FD/ON/AP/SDN
SD/MMC interface	NA
Audio feature	Support one analog audio output interface
I2C interface	Support I2C interface Comply with I2C bus protocol specification Multi host mode not supported
UART interface	• Full function serial port Baud rate support from 300bps to 3686400bps AT command and data can be sent through serial port Support RTS/CTS hardware flow control Support serial port multiplexing function conforming to GSM 07.10 protocol • Debug serial port Support debug function • UART3 serial port Ordinary two-wire serial port
USB	Compliant with USB 2.0 specification and supports slave mode but not master mode. This interface can be used for AT command sending, data transmission, software debugging and upgrading.
Firmware upgrade	Firmware upgrade via USB/FOTA
Physical characteristics	Size: 15.7*17.6*2.1mm Weight: 1.1g (Typical)
Temperature range	Normal operation temperature: -30°C to +75°C Extended operation temperature: -40°C to +85°C* Storage temperature: -45°C to +90°C

NOTE

When the module is within the extended operation temperature range, module is able to establish and maintain data transmission, SMS, etc. The performance may deviate slightly from the 3GPP specifications, but will meet 3GPP specifications again when the temperature returns to normal operating temperature levels. It is strongly recommended that customers take heat dissipation measures to ensure that the normal operating temperature of the module can't be exceeded.

2.1. Pin Assignment Overview

A7682S R5

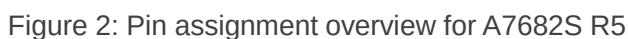


Table 5: Pin Description

PIN NO	PIN NAME	PIN NO	PIN NAME
1	TXD	2	RXD
3	RTS	4	CTS
5	DCD	6	DTR
7	RI	8	GND
9	NC	10	NC
11	SPK_P	12	SPK_N
13	GND	14	USIM_DET
15	USIM_DATA	16	USIM_CLK
17	USIM_RTS	18	USIM_VDD
19	GND	20	USB_BOOT●
21	GND	22	UART3_TXD
23	UART3_RXD	24	USB_VBUS
25	USB_DP	26	USB_DN
27	GND	28	NC
29	RESET	30	GND
31	GND	32	ANT_MAIN
33	GND	34	VBAT
35	VBAT	36	GND
37	GND	38	ADC1
39	PWRKEY	40	VDD_EXT
41	NETLIGHT	42	STATUS
43	GPIO_00	44	GPIO_01
45	GND	46	NC
47	NC	48	NC
49	NC	50	NC
51	NC	52	NC
53	NC	54	NC
55	NC	56	NC
57	GPIO_02	58	DBG_RXD
59	DBG_TXD	60	1PPS
61	NC	62	SPI_CS
63	SPI_CLK	64	SPI_MISO
65	SPI_MOSI	66	ADC2
67	GND	68	I2C_SDA
69	I2C_SCL	70	GND
71	GND	72	ANT_GNSS
73	NC	74	NC

75	NC	76	NC
77	NC	78	NC
79	NC	80	LCD_SPI_CLK
81	LCD_SPI_CS	82	LCD_RST
83	LCD_SPI_DCX	84	LCD_SPI_TXD
85	LED_K	86	GPIO_09
87	GND	88	GND
89	GND	90	GND
91	GND	92	GND

NOTE

'●' Indicates that the pin cannot be pulled down before the module powered down. Otherwise, it will affect the normal start-up of the module.

NC: NOT CONNECT. Do not connect them to GND.

2.2. Pin Description

Table 6: Pin parameter abbreviation

Pin type	Description
PI	Power input
PO	Power output
AI	Analog input
AIO	Analog input/output
I/O	Bidirectional input /output
DI	Digital input
DO	Digital output
DOH	Digital output with high level
DOL	Digital output with low level
PU	Pull up
PD	Pull down
OD	Open Drain

Table 7: 1.8V IO parameters definition

Power Domain	Parameter	Description	Min	Typ.	Max
1.8V	V _{IH}	High level input	VCC * 0.7	1.8V	VCC+0.2
	V _{IL}	Low level input	-0.3V	0V	VCC * 0.3
	R _{pu}	Pull up resistor	55KΩ	79KΩ	121KΩ
	R _{pd}	Pull down resistor	51KΩ	87KΩ	169 KΩ
	I _{IL}	Input leakage current	-	-	10uA
	V _{OH}	Output level range	VCC-0.2	-	-
	V _{OL}	Output low range	-	-	0.2V
	I _{OL}	Maximum current driving capacity at low level output Vpad=0.2V Iol DCS[1:0]=			
		00	13 mA		
		01	25 mA		
		10	37 mA		
		11	49 mA		
	I _{OH}	Maximum current driving capacity at high level output Vpad=VCC-0.2V Ioh DCS[1:0]=			
		00	11 mA		
		01	21 mA		
		10	32 mA		
		11	42 mA		

Table 8: 3.0V IO parameters definition

Power Domain	Parameter	Description	Min.	Typ.	Max.
3.0V	V _{IH}	High level input	2V	-	VCC+0.3
	V _{IL}	Low level input	-0.3V	0V	0.8V
	R _{pu}	Pull up resistor	26KΩ	47KΩ	72KΩ
	R _{pd}	Pull down resistor	27KΩ	54KΩ	267KΩ
	I _{IL}	Input leakage current	-	-	10uA
	V _{OH}	Output level range	2.4V	-	-
	V _{OL}	Output low range	-	-	0.4V
	LOL	Maximum current driving capacity at low level output Vpad=0.4V			

		Iol DS[2:0]= 000 001 010 011 100 101 110 111	7 mA 10 mA 14 mA 18 mA 21 mA 24 mA 28 mA 31 mA
	LOH	Maximum current driving capacity at high level output Vpad=VCC-0.5V loh DS[2:0]= 000 001 010 011 100 101 110 111	7 mA 10 mA 13 mA 16 mA 19 mA 23 mA 26 mA 29 mA

Table 9: Pin description

Pin name	Pin No.	Pin parameter		Description	Note
		Power domain	Type		
Power supply					
VBAT	34,35	-	PI	Module input voltage ranges from 3.4V to 4.2V, typical values is 3.8V.	
VDD_EXT	40	-	PO	1.8V power output, output current up to 50 mA.	Default on. If unused, keep it open.
GND	8,13,19,21,27,30,31,33,36,37,45,67,70,71,87,88,89,90,91,92	-	-	Ground	
System Control					
PWRKEY	39	-	DI,PU	Power ON/OFF input,	Default high

				active low.	VIH: 0.7*VBAT VIL: 0.3*VBAT PMU has been internally pulled up to the VBAT with 50K (Typical).
RESET	29	-	DI,PU	System reset control input, active low.	Default high VIH: 0.7*VBAT VIL: 0.3*VBAT PMU has been internally pulled up to the VBAT with 50K (Typical).

USIM interface

USIM_DET	14	1.8V	DI	USIM card insert detect.	It can be set to high/low active with the AT command, refer to Document [18].
USIM_DATA	15	1.8/3.0V	DIO	USIM data signal.	This pin has been pull-up with 4.7KΩ resistor to USIM_VDD internally.
USIM_CLK	16	1.8/3.0V	DO	USIM clock signal.	
USIM_RST	17	1.8/3.0V	DO	USIM reset signal.	
USIM_VDD	18	1.8/3.0V	PO	USIM card power supply output.	The voltage can be dynamically changed according to the type of external card, output current maximum 50mA.

USB interface

VBUS	24	-	PI	Valid USB detection input. Active high, $V_{min}=3.0V$, $V_{max}=5.2V$, $V_{norm}=5V$.	
USB_DN	26	-	AIO	Negative electrode of the differential, bi-directional USB signal.	
USB_DP	25	-	AIO	Positive electrode of the differential, bi-	

				directional USB signal.	
Full function UART interface					
TXD	1	1.8V	DOH	Data output	If unused, keep it open.
RXD	2	1.8V	DI	Data input	
RTS	3	1.8V	DI	RTS input	Connect to the RTS of DTE. If unused, keep it open.
CTS	4	1.8V	DO	CTS output	Connect to the CTS of DTE. If unused, keep it open.
DCD	5	1.8V	DO	Carrier detection	If unused, keep it open.
DTR	6	1.8V	DI	DTE Ready	
RI	7	1.8V	DO	Ringing indicator	
Debug UART					
DEBUG_RXD	58	1.8V	DI	Debug UART, the boot log will be output during boot up.	Default used as debug port.
DEBUG_TXD	59	1.8V	DOH		
Serial Port UART3					
UART3_TXD	22	1.8V	DO	Data output	Two-wire serial port
UART3_RXD	23	1.8V	DI	Data input	
SPI interface					
SPI_CS	62	1.8V	DO	SPI CS	If unused, keep it open.
SPI_CLK	63	1.8V	DO	SPI clock	
SPI_MISO	64	1.8V	DI	SPI master input slave output	
SPI_MOSI	65	1.8V	DO	SPI master output slave input	
LCD interface					
LCD_SPI_CLK	80	1.8V	DO	LCD dedicated SPI clock	If unused, keep it open.
LCD_SPI_CS	81	1.8V	DO	LCD special SPI chip selection	
LCD_RST	82	1.8V	DO	LCD reset	
LCD_SPI_DCX	83	1.8V	DO	LCD special SPI data cable	
LCD_SPI_TXD	84	1.8V	DIO	LCD special SPI data cable	
LED_K	85	1.8V	AO	LCD backlight SINK adjustment	

I2C interface					
I2C_SDA	68	1.8V	OD	I2C data IO	If unused, keep it open. Need pull up to VDD_EXT.
I2C_SCL	69	1.8V	OD	I2C clock output	
Analog audio interface					
SPK_P	11	-	AO	Audio receiver output positive	If unused, keep it open.
SPK_N	12	-	AO	Audio receiver output negative	
GPIO					
GPIO_00	43	1.8V	IO,PU	General purpose I/O	If unused, keep it open.
GPIO_01	44	1.8V	IO,PD	General purpose I/O	
GPIO_02	57	1.8V	IO,PD	General purpose I/O	
GPIO_09	86	1.8V	IO,PU	General purpose I/O	
ANT interface					
ANT_MAIN	32	-	AIO	Main antenna	
ANT_GNSS	72		AIO	GNSS antenna	
Other pins					
ADC1	38	-	AI	General Purpose ADC	Voltage input range 0-1.2 V.
ADC2	66		AI	General Purpose ADC	Voltage input range 0-1.2 V.
NETLIGHT	41	1.8V	DO	Network registration status indicator (LED).	
STATUS	42	1.8V	DO	Module status indicator (LED).	
USB_BOOT●	20	1.8V	DI	Firmware download guide control input. When pull-down to GND and press PWRKEY, module will access in USB download mode.	It is recommended to place a test point for easy debugging and upgrade. Do not pull down before normal boot.

NOTE

1. Please reserve a test point for USB_BOOT, GND, DEBUG_TXD and VDD_EXT. If there is no USB connector, please also reserve a test point for USB_VBUS, USB_DP, and USB_DN for firmware upgrading.
2. '●' Indicates that the pin cannot be pulled down before the module powered on. Otherwise, it will affect the normal start-up of the module.

The following figure shows the package outline drawing of A7682S R5.



The side length dimension is 15.70*17.60±0.15mm excluding the burr area.

3. Interface Application

3.1. Power Supply

The module offers 2 power supply pins (34, 35) as VBAT power input pin. A7682S R5 supplies power to the internal RF and baseband circuits through these two pins.

When the module is transmitting at maximum power in LTE mode, the current can reach up to a peak current, please ensure that the external power supply capacity is no less than 1A.

Table 10: Power interface pins definition

Pin name	Pin No.	Type	Description	Note
VBAT	34,35	PI	Module power input	The input voltage range is 3.4V~4.2V, and the external power supply needs to provide a current carrying capacity of 1A.
GND	8,13,19,21,27,30,31,33,36,37,45,67,70,71,87,88,89,90,91,92			

Table 11: VBAT pins electronic characteristic

Parameter	Description	Min.	Typ.	Max.	Unit
VBAT	Module supply voltage	3.4	3.8	4.2	V
I _{VBAT} (peak)	Module consumption peak current	-	-	700	mA
I _{VBAT} (average)	Module average consumption current (idle mode)	-	11	-	mA
I _{VBAT} (sleep)	Current in Sleep mode@DRX=0.32S	-	1.22	-	mA
	Current in Sleep mode@DRX=0.64S	-	0.92	-	mA
	Current in Sleep mode@DRX=1.28S	-	0.72	-	mA
	Current in Sleep mode@DRX=2.56S	-	0.61	-	mA
I _{VBAT} (PSM)	Current in PSM mode	-	8	-	uA
I _{VBAT} (power-off)	Module average consumption current (off leakage current)	-	7	-	uA

NOTE

Test condition: VBAT power supply 3.8V, the module is tested on EVB board, and the power input has a 200uF tantalum capacitor.

3.1.1. Power Supply Design Guide

In the customer's design, special attention must be paid to the design of the power supply. If the voltage drops below 3.4V, the RF performance of the module will be affected, the module will shut down if the voltage is too low. It is recommended to select an LDO or DC-DC chip with an enable pin, and the enable pin is controlled by the MCU.

NOTE

When the power supply can provide a continuous current of 1A, the total capacity of the external power supply capacitor is recommended to be no less than 200uF.

It is recommended to place four 10pF/33pF/0.1uF/1uF ceramic capacitors near VBAT to improve RF performance and system stability. At the same time, it is recommended that the VBAT layout routing width from the power supply on the PCB to the module be at least 2mm. The recommended reference design is as follows:

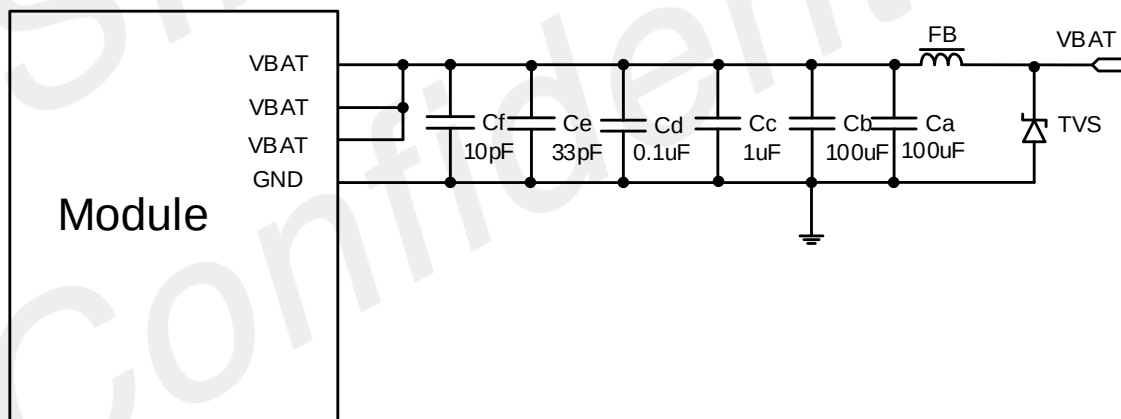


Figure 4: Power supply application circuit

If the VBAT input contains high-frequency interference, it is recommended to add magnetic beads for filtering. The recommended types of magnetic beads are BLM21PG300SN1D and MPZ2012S221A.

In addition, in order to prevent the damage of A7682S R5 caused by surge and overvoltage, it is recommended to parallel one TVS on the VBAT pin of the module.

Table 12: TVS for VBAT part number list

Manufacturer	Part Number	V_{RWM}	$V_C(Max)$	$P_{PP}(Max)$	$C_J(Max)$	Package
WILL	ESD56301D05-2/TR	5V	9.5V	1500W	700pF	DFN1610-2L
WILL	ESD56301D04-2/TR	4.85V	11V	2000W	480pF	DFN1610-2L
WAYON	WS2057KP	5V	12V	2040W	700pF	DFN1610-2L
WAYON	WS4.5DPHXM	4.85V	11V	2255W	700pF	DFN1610-2L

NOTE

When selecting TVS by customer, it is necessary to pay attention to the clamping voltage in the case of surge protection. The clamping voltage should not be higher than 10V when 100V surge input.

3.1.2. Recommended Power Supply Circuit

In order to avoid damaging the module, please do not cut off the power supply when module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.

It is suggested that customer's design should have the ability to cut off the power supply for module in abnormal state, and then switch on the power supply to restart the module.

When the input power is greater than 5V, it is recommended to use DCDC chip. When the input is less than 5V, use the LDO power supply. If the OPEN LINUX secondary development function of the module is used, since there is no MCU, a low-cost MCU can be added to play the role of the hardware watchdog that can pull PWRKEY to start up and power off.

It is recommended that a switching mode power supply is used. The following figure shows the DC-DC regulator reference circuit:

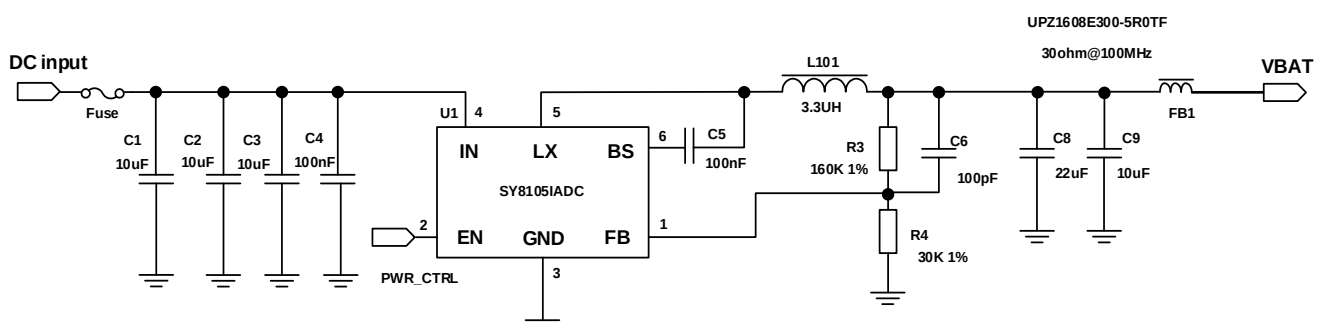


Figure 5: Power supply reference circuit

When the VBAT power is turned off, the voltage should decrease rapidly within 50ms. To avoid voltage anomalies, when the VBAT is lower than the minimum value, the system must power on the VBAT at a voltage which lower than 100mV for at least 2 second to restart the system.

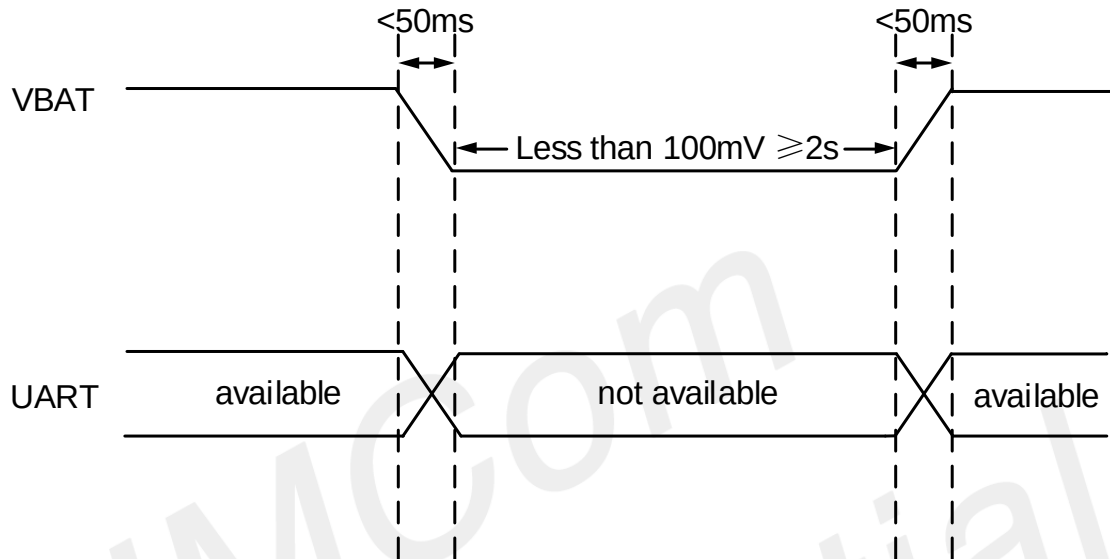


Figure 6: Power-off and power-on restart sequence

3.1.3. Voltage Monitor

AT command 'AT+CBC' can be used to monitor VBAT voltage.

AT command 'AT+CVALARM' can be used to set high/low voltage alarm, when the actual voltage exceeds the preset range, a warning message will be reported through the AT port.

AT command 'AT+CPMVT' can be used to set high/low voltage power off, when the actual voltage exceeds the preset range, the module will shut down automatically.

NOTE

Overvoltage alarm and overvoltage shutdown are off by default. For details of AT commands, please refer to document [1].

3.2. Power On/ Off and Reset

3.2.1. Power on

Table 13: PWRKEY interface pin definition

Pin name	Pin No.	Type	Description	Note
PWRKEY	39	DI,PU	Power ON/OFF input, active low.	PMU has been internally pulled up to the VBAT with 50K (Typical).

Customer can power on the module by pulling down the PWRKEY pin. It is recommended to add TVS diode near the module pin for ESD performance. The recommended circuit is as follows:

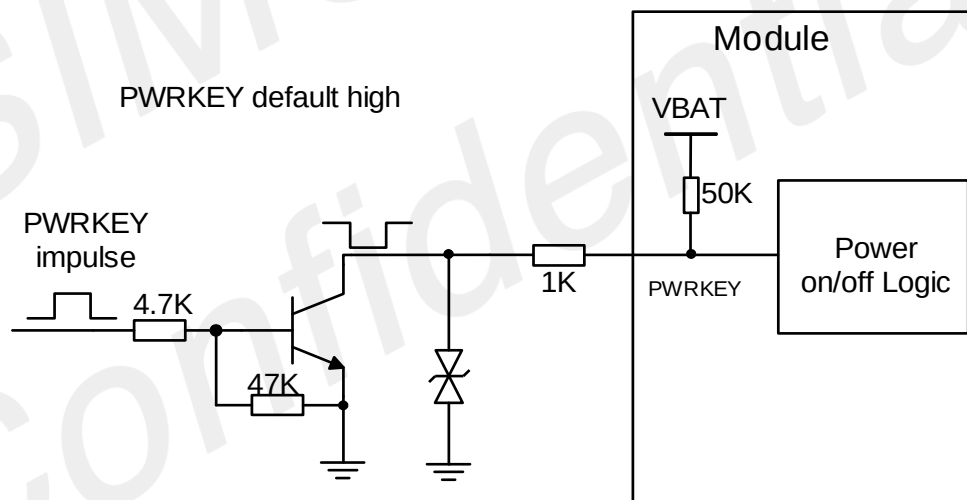


Figure 7: Reference power on/off circuit

NOTE

1. It is forbidden to pull down both RESET key and PWRKEY to power on the module at the same time.
2. If the customer does not need to start the PWRKEY automatically, do not connect a capacitor larger than 10pF on the PWRKEY and RESET. Otherwise, the module will start automatically if the low level is detected during the power-on.

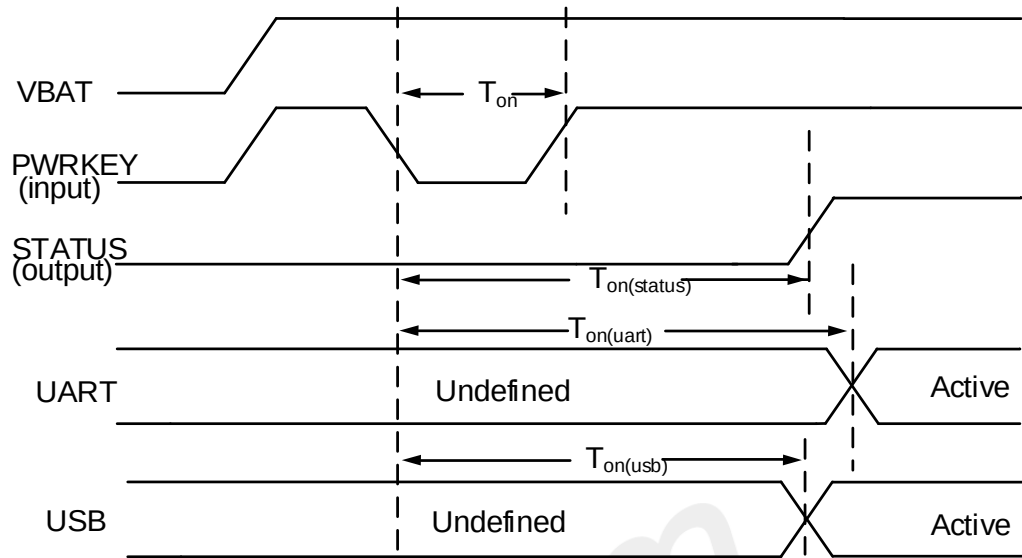


Figure 8: Power on sequence

Table 14: Power on timing and electronic characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{on}	The time of active low-level impulse of PWRKEY pin to power on module	-	50	-	ms
$T_{on(status)}$	The time from power-on issue to STATUS pin output high level (indicating power up ready)	-	7	-	s
$T_{on(uart)}$	The time from power-on issue to UART port ready	-	9	-	s
$T_{on(usb)}$	The time from power-on issue to USB port ready	-	8	-	s
V_{IH}	Input high level voltage on PWRKEY pin	$0.7 \cdot V_{BAT}$	-	V_{BAT}	V
V_{IL}	Input low level voltage on PWRKEY pin	0	0	$0.3 \cdot V_{BAT}$	V

3.2.2. Power off

The following methods can be used to power off the module.

- Power off by pulling the PWRKEY pin down to a low level for 2.5s.
- Power off Module by AT command 'AT+CPOF'.
- Over-voltage or under-voltage automatic power off, the voltage range can be set by 'AT+CPMVT'.
- Over-temperature or under-temperature automatic power off.

It is strongly recommended that the customer use PWRKEY or 'AT+CPOF' to shut down, and then cut off VBAT (especially when the module does not need to work). In addition, the customer cannot shut down VBAT by disconnecting it, which may cause damage to flash.

NOTE

When the temperature exceeds the range of $-30 \sim +75^{\circ}\text{C}$, A7682S R5 will report warning information through AT port. When the temperature exceeds the range of $-40 \sim +85^{\circ}\text{C}$, A7682S R5 will shut down automatically. For a detailed description of 'AT+ CPOF' and 'AT+ CPMVT', please refer to document [1].

PWRKEY can be used to power off the module. For power off sequence, please see the following figure:

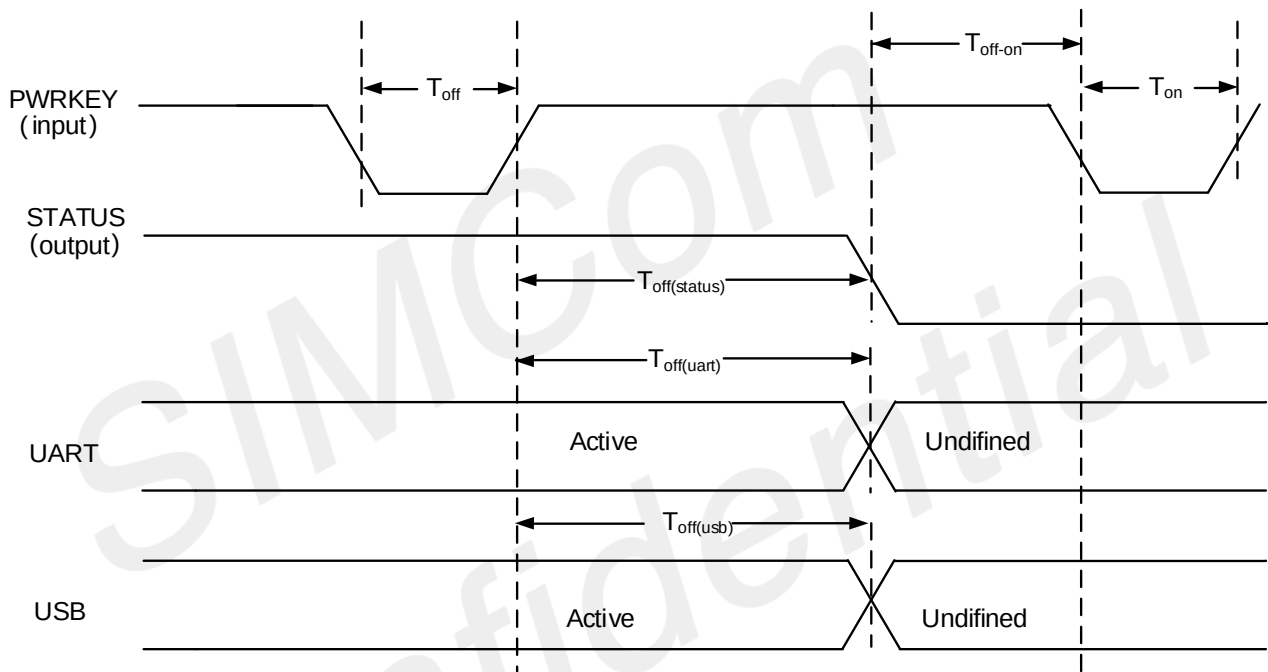


Figure 9: Power off timing sequence

Table 15: Power off sequence parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{off}	Power off low level pulse width	2.5	-	-	s
$T_{off(status)}$	Power off time (according to status interface)	-	2.5	-	s
$T_{off(usb)}$	Power off time (according to UART interface)	-	2.5	-	s
$T_{off(usb)}$	Power off time (according to USB interface)	-	2.5	-	s
T_{off-on}	Power off - power on buffer time	2	-	-	s

NOTE

The status pin can be used to judge whether the module is powered on or not. When the module is powered on and initialization is completed, the status outputs a high level. Otherwise, the low level will be maintained all the time.

3.2.3. Reset Function

Table 16: RESET interface pin definition

Pin name	Pin No.	Type	Description	Note
RESET	29	DI,PU	System reset control input, active low. VIH: 0.7*VBAT VIL: 0.3*VBAT	PMU has been internally pulled up to the VBAT with 50K (Typical).

The module can be reset by pulling down the reset pin to a low level. It is recommended to add TVS diode near the module pin for ESD performance. The recommended circuit is shown as follows:

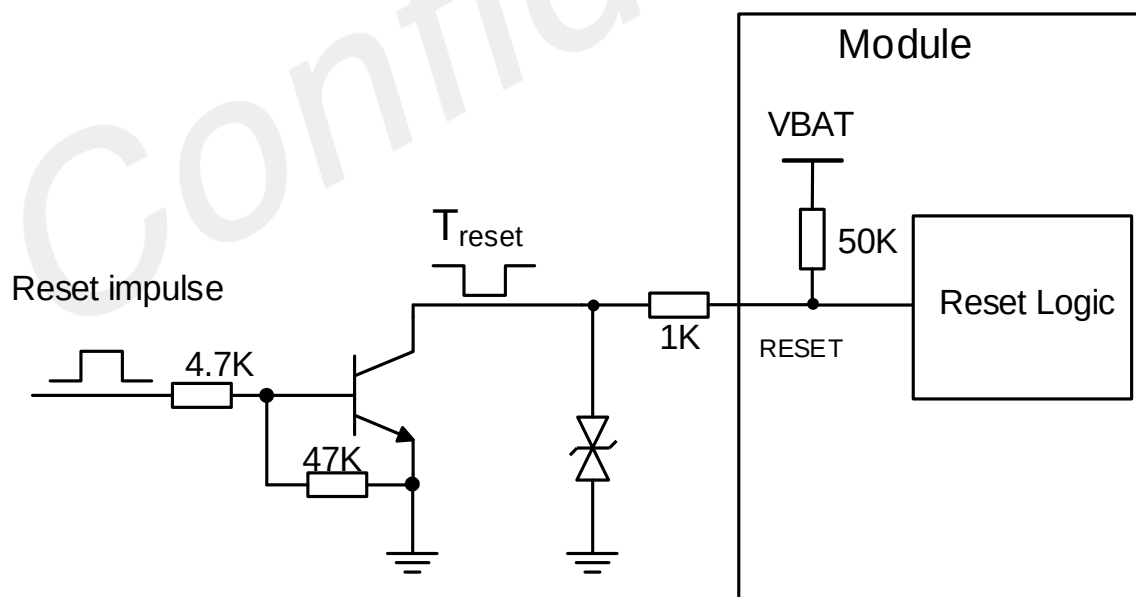


Figure 10: Reference reset circuit

Table 17: RESET pin electronic characteristic

Symbol	Description	Min.	Typ.	Max.	Unit
T_{reset}	The active low level time impulse on RESET pin to reset module	2	2.5	-	s
V_{IH}	Input high level voltage	$0.7 \cdot V_{BAT}$	-	V_{BAT}	V
V_{IL}	Input low level voltage	0	0	$0.3 \cdot V_{BAT}$	V

NOTE

1. It is recommended to use the reset pin only in case of emergency, such as the module is not responding. The reset time is recommended to be 2.5s.
2. Do not connect a capacitor larger than 10pF on the PWRKEY and RESET. Otherwise, the module will start automatically if the low level is detected during the power-on.

3.3. UART Interface

The module provides three serial ports, the main communication serial port is MAIN_UART, one ordinary serial port for peripherals communication, and the DEBUG_UART dedicate to print log.

Table 18: UART information

Interface Type	Support Baud Rate (bps)	Default Baud Rate (bps)	Function Description
Full function UART	300 600 1200 2400 4800 9600 19200 38400 57600 115200 230400 460800 921600 1842000 and 3686400	115200	Data transmission and AT command transmission
Debug UART	115200	115200	Module partial log output
Two-wire UART	115200	115200	Used to communicate with peripherals

Table 19: UART interface pins definition

Pin name	No.	Power domain	Type	Description	Note
Full function UART interface					
TXD	1	1.8V	DOH	Data output	If unused, keep it open.

RXD	2	1.8V	DI	Data input	
RTS	3	1.8V	DI	DTE request sent	Connect to the RTS of DTE. If unused, keep it open.
CTS	4	1.8V	DO	DTE clears sending	Connect to the CTS of DTE. If unused, keep it open.
DCD	5	1.8V	DO	Carrier detection	If unused, keep it open.
DTR	6	1.8V	DI	DTE Ready	
RI	7	1.8V	DO	Ringing indicator	

Debug UART

DEBUG_TXD	59	1.8V	DOH	Debug UART, the boot log will be output during boot up.	Default used as debug port.
DEBUG_RXD	58	1.8V	DI		

UART3

UART3_TXD	22	1.8V	DOH	Data output	Two-wire serial port
UART3_RXD	23	1.8V	DI	Data input	

NOTE

It is recommended that the baud rate of the serial port without the flow control function not exceed 921600.

3.3.1. UART Design Guide

When customer uses full-function serial port, please refer to the following connection mode:

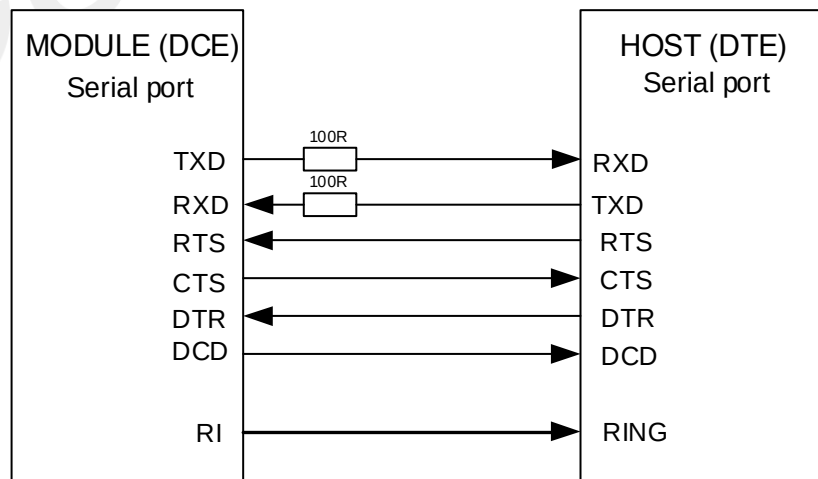


Figure 11: Serial port connection diagram (Full-function mode)

When using 2-wire serial port, please refer to the following connection mode:

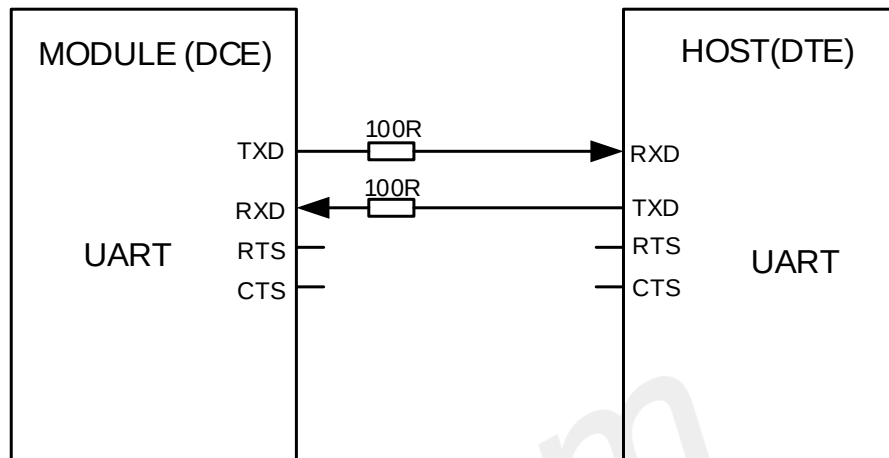


Figure 12: Serial port connection diagram (NULL mode)

The following figure shows the use of triode for level shifter circuits. Please pay special attention to the direction of signal.

The recommended triode model is MMBT3904.

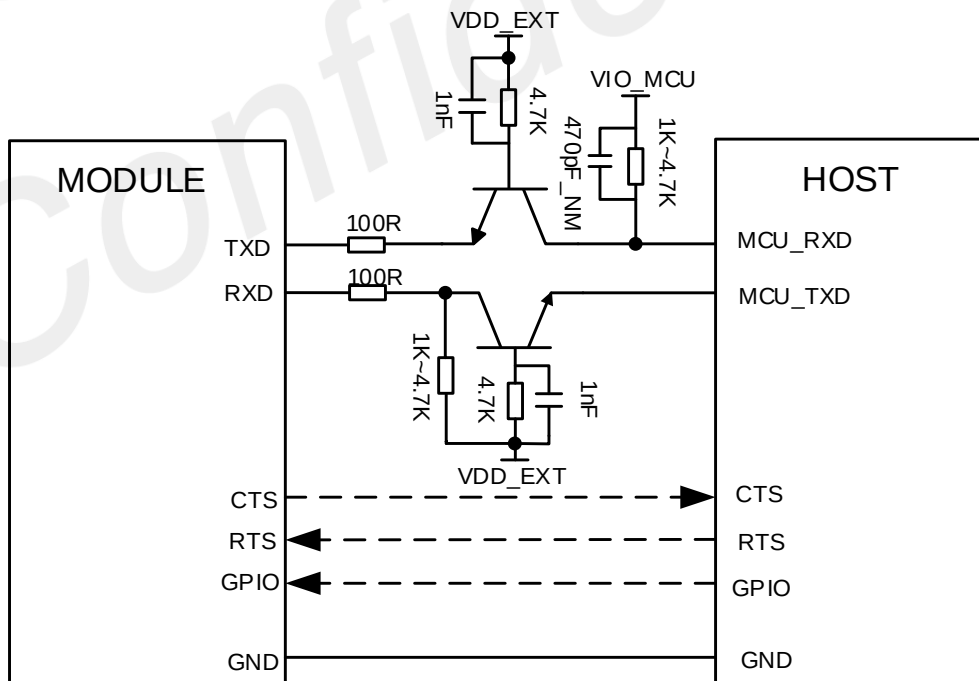


Figure 13: Triode level conversion circuit

NOTE

1. The parasitic capacitance of the transistor will affect the edge of the high-speed digital signal. It is not recommended to use this circuit when the signal speed is higher than 115200bps.
2. It is recommended that the TXD and RXD are connected with 100R resistors in series on the module end to prevent damage to module pins caused by static electricity or surge.

3.3.2. RI and DTR Behavior

RI usually keeps high level output. When receiving a short message or URC report, RI outputs a low level for 120ms (short message)/60ms (URC), and then returns to a high-level state.

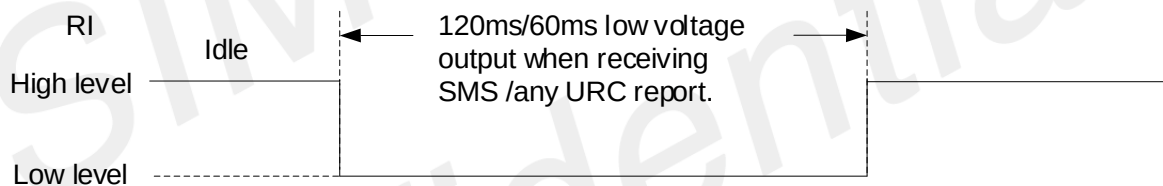


Figure 14: RI behaviour (SMS and URC report)

3.3.3. DTR Function Description

The DTR can be used as the sleep-wake pin of the module. After the module enters sleep mode, pull down the DTR to wake up the module. DTR defaults to high level.

When the customers set "AT+CSCLK=1", the module will automatically enter sleep mode. After entering sleep mode, the serial port function cannot communicate normally, and external pulling down the DTR can wake up the module.

After setting the AT command "AT+CSCLK=0", pulling the DTR pin to a high level will not have any effect, and the normal communication of the serial port function will not be affected.

3.4. USB Interface

The module contains a USB interface, which complies with the USB2.0 specification as a peripheral, but does not support USB charging function and USB HOST mode.

USB supports high speed mode (480Mbps) and full speed mode (12Mbps), it is used for AT command communication, data transmission, firmware upgrade and software debugging.

Table 20: USB interface pins definition

Pin name	No.	Power domain	Type	Description	Note
VBUS	24	-	PI	Valid USB detection input. Active high, $V_{min}=3.0V$, $V_{max}=5.2V$, $V_{norm}=5.0V$	
USB_DP	25	-	AIO	Positive electrode of the differential, bi-directional USB signal.	
USB_DN	26	-	AIO	Negative electrode of the differential, bi-directional USB signal.	

3.4.1. USB Reference Design

USB is the main debugging port and software upgrade interface. It is recommended that customers reserve USB test points for debugging during design. If a main control chip is connected, 0R resistors must be reserved for switching external test points during design. The recommended reference design is as follows:

The branch wiring should not exceed 2mm

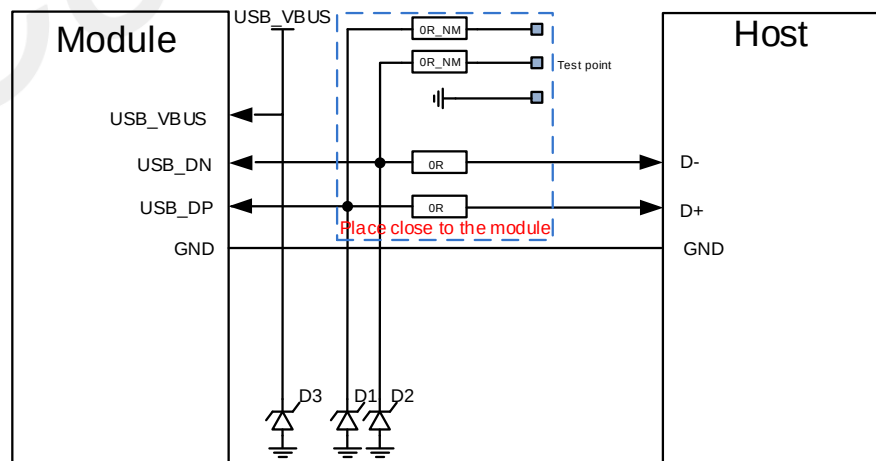


Figure 15: USB circuit diagram

Customers should pay attention to the selection of D3 devices. It is recommended to choose anti-static and anti-surge two-in-one devices, and one TVS tube can be placed, recommended model AZ9707-01F. D+/D- trace impedance is controlled according to 90Ω and covered with ground; D1/D2 select TVS tube with capacitance value <1pf, and they should be placed near the USB connector or test point, recommended models ESD73131CZ and ESD9L5.0ST5G.

USB_VBUS is the USB detection pin for module, it's active high and the available identification voltage is 3.0V~5.2V, generally recommend to connect to the VBUS signal of external USB connector or of MCU, it also can be connected to other power supplies, such as the VBAT. If the USB_VBUS pin is connected to the power supply, it's recommended to reserve a switch circuit to ensure that the power supply can be turned off then turn it on, that make USB enumerating afresh.

Table 21: TVS for USB part number list

Manufacturer	Part Number	V _{RWM}	V _C (Max)	C _J (Max)	Package
WILL	ESD73131CZ-2/TR	5V	6.5V	0.45pF	DWN0603-2L
ON	ESD9L5.0ST5G	5V	9.8V	0.9pF	SOD-923
NXP	PESD5V0F1BSF	5V	10V	0.3pF	DSN0603-2
AMAZING	AZ9707-01F	7V	12.5V	950pF	DFN1610

NOTE

1. The USB data cable must be strictly routed in 90Ω differential. The TVS devices D1 and D2 on the data line must be selected with equivalent capacitance less than 1pF. TVS should be placed near USB connectors or test points, and the recommended models are ESD73131CZ, ESD9L5.0ST5G, or PESD5V0F1BSF.
2. Route away from other sensitive signals (RF, audio, and XO).
3. The USB 2.0 speed detection is automatically determined through the USB protocol. Customer does not need to additionally pull up the DP. Otherwise, it may affect the USB enumeration of the module.

3.4.2. USB_BOOT Interface

The module provides one forced download boot interface 'USB_BOOT'.

Table 22: USB_BOOT interface pin definition

Pin name	No.	Power domain	Type	Description	Note
USB_BOOT	20	1.8V	DI	Firmware download guide control input. When pull-down to GND and press PWRKEY, module will access in USB download mode.	Please reserve 2 test points for debug. Do not pull down USB_BOOT during normal power on!

If the module fails to boot, customers can force upgrade through the USB_BOOT port.

Before the module is powered on, pull down the USB_BOOT pin to GND, then apply VBAT power to the module, and press PWRKEY to enter the download mode. After entering the download mode, release USB_BOOT and remove the pull-down.

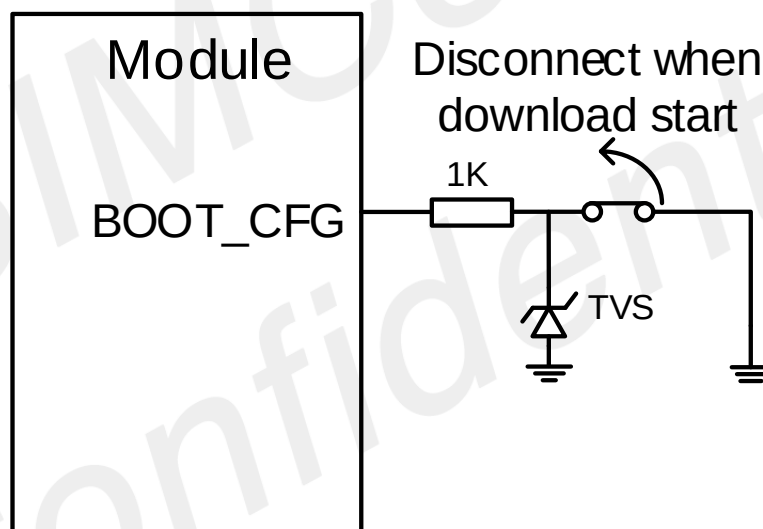


Figure 16: Reference USB_BOOT circuit

Customers will see the download port in the device manager port of the windows system.

Force-download port:



The port after powering on normally:

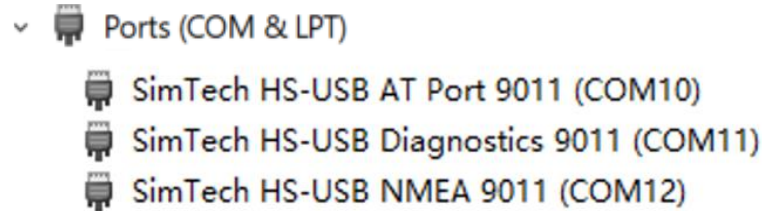


Figure 17: The USB port

NOTE

1. USB_BOOT is the download control pin, this pin cannot be pulled down before the normal power on. Otherwise, it will enter the download mode.
2. It is recommended to reserve test point to facilitate debugging and upgrading.

3.5. USIM Interface

The module supports both 1.8V and 3.0V USIM cards. The interface power of the USIM card is provided by the voltage regulator inside the module.

Table 23: USIM interface pins definition

Pin name	No.	Power domain	Type	Description	Note
USIM_DET	14	1.8V	DO	USIM card insert detect.	It can be set to high/low active with the AT command, refer to Document [18].
USIM_DATA	15	1.8/3.0V	DIO	USIM data signal.	This pin has been pulled up with 4.7KΩ resistor to

					USIM_VDD internally.
USIM_CLK	16	1.8/3.0V	DO	USIM clock signal.	
USIM_RST	17	1.8/3.0V	DO	USIM reset signal.	
USIM_VDD	18	1.8/3.0V	PO	USIM card power supply output.	The voltage can be dynamically changed according to the type of external card, output current maximum 50mA.

Table 24: USIM electronic characteristic in 1.8V mode (SIM_VDD=1.8V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SIM_VDD	LDO power output voltage	1.62	1.8	1.98	V
V _{IH}	High-level input voltage	0.7*SIM_VDD	-	SIM_VDD+0.4	V
V _{IL}	Low-level input voltage	-0.4	0	0.25*SIM_VDD	V
V _{OH}	High-level output voltage	SIM_VDD-0.4	-	SIM_VDD	V
V _{OL}	Low-level output voltage	-	0	0.2	V

Table 25: USIM electronic characteristic in 3.0V mode (SIM_VDD=3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SIM_VDD	LDO power output voltage	2.7	3	3.3	V
V _{IH}	High-level input voltage	0.7*SIM_VDD	-	USIM_VDD+0.4	V
V _{IL}	Low-level input voltage	-0.4	0	0.25*SIM_VDD	V
V _{OH}	High-level output voltage	SIM_VDD-0.45	-	SIM_VDD	V
V _{OL}	Low-level output voltage	-	0	0.3	V

3.5.1. SIM Hot Swap Function

The (U)SIM card supports the hot swap function. You can use AT+UIMHOTSWAPON=1 to turn on the hot swap detection function.

If the (U)SIM card holder is of the normally open type, the AT command “AT+UIMHOTSWAPLEVEL=0” can be sent to set the detection level to a low level, when SIM_DET is pulled down, the (U)SIM card is considered inserted.

If the (U)SIM card holder is of the normally closed type, the AT command “AT+UIMHOTSWAPLEVEL=1” can be sent to set the detection level to a high level, when SIM_DET is pulled up, it is considered that the (U)SIM card is inserted.

For more detailed information on (U)SIM card AT operation, please refer to the document [1]. If the (U)SIM card hot swap function is not used, the customer can maintain the SIM_DET pin is disconnected.

3.5.2. SIM Application Guide

It is recommended to use ESD protection component. Note that the USIM peripheral circuit should be close to the USIM card socket. The following figure shows the 6-pin SIM card holder reference circuit.

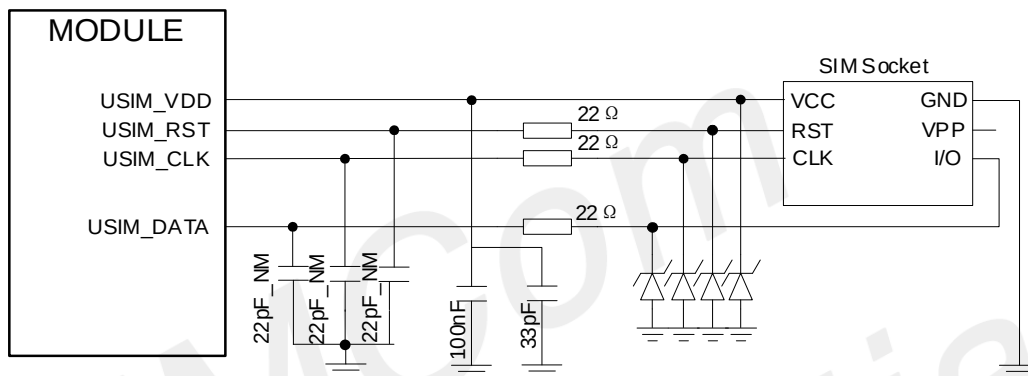


Figure 18: SIM interface reference circuit

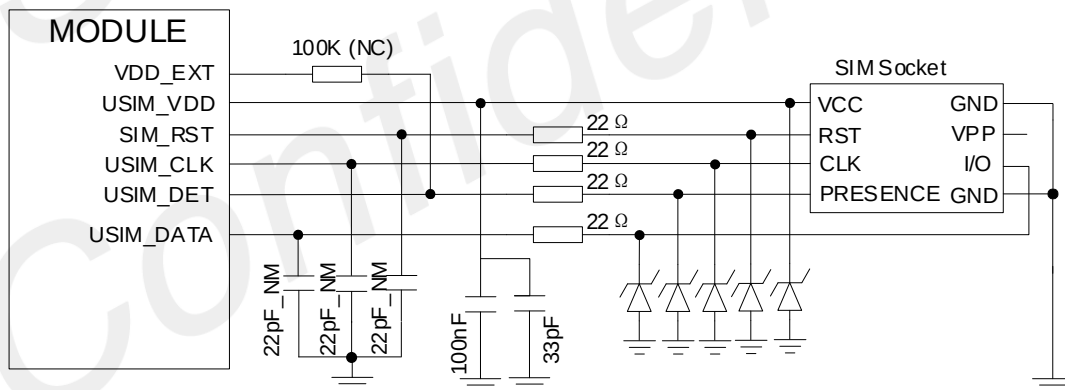


Figure 19: SIM interface reference circuit (8PIN)

NOTE

1. USIM_DATA has been pulled up with a 4.7KΩ resistor to USIM_VDD in module.
2. A 100nF capacitor on USIM_VDD is used to reduce interference.
3. For more details of AT commands about USIM, please refer to document [1].

The circuit of the USIM card is easy to be interfered with, resulting in the failure to recognize or drop the card, etc. so please follow the following principles during the design:

- Be sure to keep the USIM socket away from the main antenna during the PCB layout phase.
- USIM card traces should be away from RF, VBAT and high speed signals, at the same time the USIM card traces should be as short as possible.
- Keep the USIM socket's GND pin directly connected to the main ground.
- To prevent USIM_CLK from other signal interference, it is suggested to make separate package to protect USIM_CLK processing.
- Place TVS near the USIM socket, and the parasitic capacitance of TVS should not be greater than 15pF, such as WS03DTUMS-B.
- Connect 22 Ω resistors in series between USIM socket and module can enhance ESD protection performance.
- The rise/fall time of USIM_CLK should not exceed 40ns.

Table 26: TVS for USIM socket part number list

Manufacturer	Part Number	V _{RWM}	V _C (Max)	P _{PP} (Max)	C _J (Max)	Package
WAYON	WS03DTUMS-B	3.3V	8V	35W	0.7pF	DFN0603-2L
WILL	ESD9X5VU-2/TR	5V	8V	72W	0.9pF	DFN1006-2L

3.6. SPI Interface

The module provides a set of 4 wire SPI interface with maximum clock rate of 52MHz. It supports master mode and provides full-duplex format, synchronous and serial communication with peripheral devices.

Table 27: SPI interface pins definition

Pin name	No.	Power domain	Type	Description	Note
SPI_CS	62	1.8V	IO	SPI chip select signal	If unused, keep it open.
SPI_CLK	63	1.8V	IO	SPI clock	
SPI_MISO	64	1.8V	IO	SPI master input slave output	
SPI_MOSI	65	1.8V	IO	SPI master output slave input	

The recommended reference design is as follows:

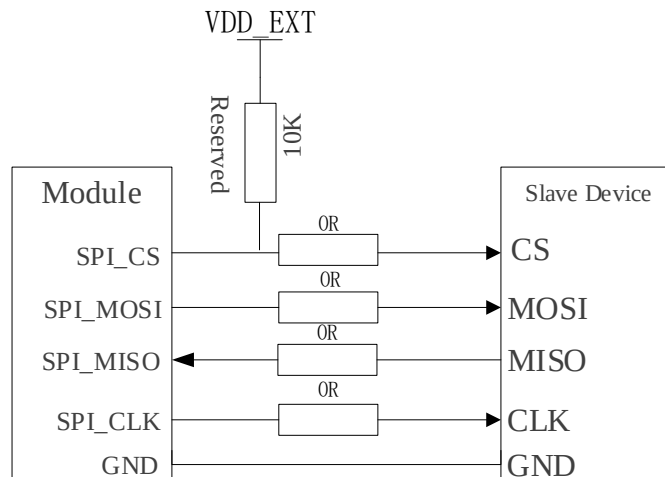


Figure 20: SPI reference circuit

3.7. Audio Interface

3.7.1. Analog Audio Onput Interface

The module provides an analog audio output interface, which can be connected to an external speaker for multimedia playback.

Table 28: Analog audio output interface definition

Pin name	No.	Power domain	Type	Description	Note
SPK_P	11	-	AO	Analog audio output channel (+)	If unused, keep it open.
SPK_N	12	-	AO	Analog audio output channel (-)	

3.7.2. Analog Audio Reference Design

The recommended reference design is as follows:

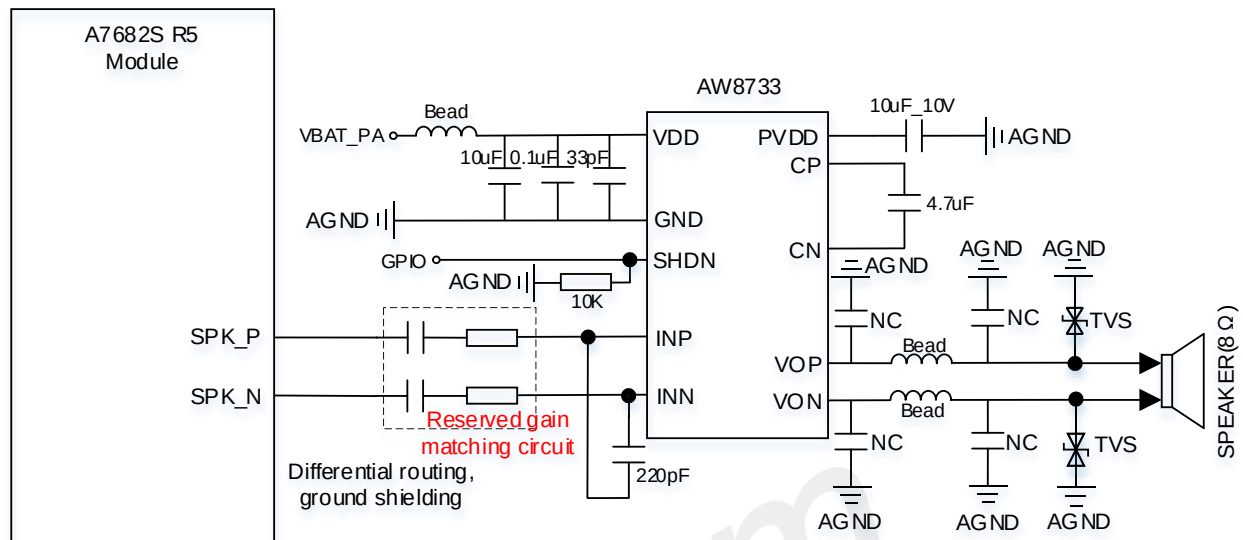


Figure 21: Analog audio reference circuit

3.8. I2C Interface

The module provides one I2C interface, which supports standard speed clock frequency 100Kbps and high speed clock frequency 400Kbps. Its operation voltage is 1.8V.

Table 29: I2C interface pins definition

Pin name	No.	Power domain	Type	Description	Note
I2C_SCL	69	1.8V	OD	I2C clock output	If unused, keep it open. Need to pull up to VDD_EXT.
I2C_SDA	68	1.8V	OD	I2C data I/O	

The recommended reference design is as follows:

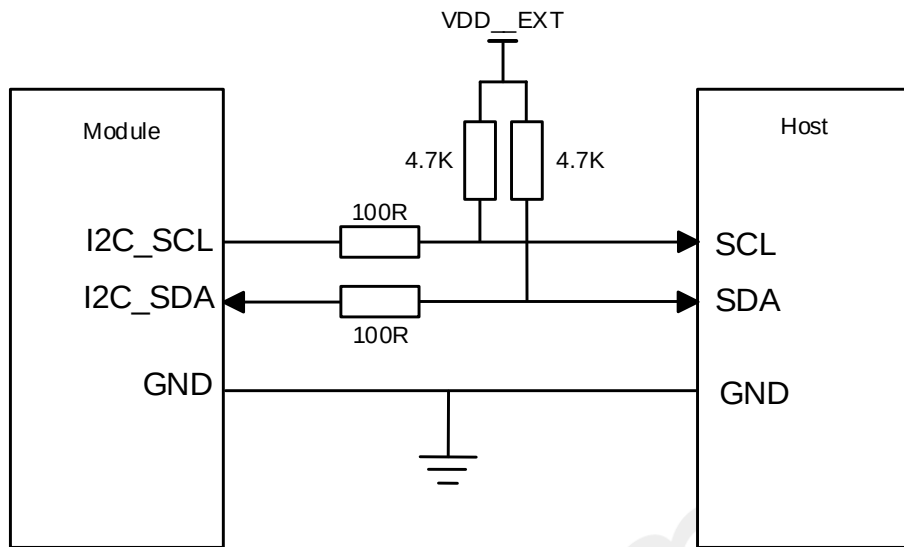


Figure 22: I2C reference circuit

NOTE

1. The SCL and SDA pins require pull-up resistors, and the pull-up power supply must be VDD_EXT of the module output.
2. Connecting a 100R resistor in series with the I2C signal line close to the module terminal is recommended to reduce overshoot on the signal line.

3.9. LCD Interface

Module supports LCD interface, only support the LCD module with 1 data line, the LCD interface of the module has no special LCD_TE signal pin, if necessary, you can choose GPIO to simulate the use, it is recommended to use the GPIO_02 as the LCD_TE signal.

It is recommended that the voltage stabilizer capacitor and decoupling capacitor be reserved on the LCD power supply line, and the 0Ω resistance in series be reserved for commissioning. At the same time, the data line is also reserved in series 0Ω resistance to facilitate the adjustment of signal quality, to prevent signal reflection, overshoot and other phenomena.

Table 30: LCD interface description

Pin Name	Pin No	I/O	Description	Note
LCD_SPI_CLK	80	DO	LCD dedicated SPI clock	
LCD_SPI_CS	81	DO	LCD special SPI chip selection	
LCD_RST	82	DO	LCD reset	
LCD_SPI_DCX	83	DI	LCD special SPI data cable	
LCD_SPI_TXD	84	DIO	LCD special SPI data cable	
LED_K	85	DI	LCD backlight SINK adjustment	

NOTE

Module supports LCD backlight SINK adjustment. As a current sink pin, it can be directly connected to the LEDK pin of LCD, and the backlight can be adjusted by configuring the SINK through SW. The sink current range is 3mA~96mA, step=3mA, and the peripheral MOS tube drive circuit can be omitted. Due to chip space limitations, it is necessary to cut some other functions to implement this function, if you need it, please contact the SIMCom support team

3.10. GPIO Interface

The module provides multiple GPIOs.

Table 31: Standard GPIO Resources of A7682S R5

Pin No.	Pin name	AT command operation GPIO number	Pin typ.	Power domain	Default function	Pad Edge wakeup
43	GPIO_00	GPIO0	IO,PD	1.8V	GPIO	YES
44	GPIO_01	GPIO1	IO,PD	1.8V	GPIO	YES
57	GPIO_02	GPIO2	IO,PD	1.8V	GPIO	YES
86	GPIO_09	GPIO9	IO,PD	1.8V	GPIO	YES

3.11. STATUS Interface

The STATUS pin can be used to determine whether the module is powered on or not. When the module is powered on and initialization is complete, the status output is high. Otherwise, it will remain low.

Table 32: STATUS interface pin definition

Pin name	No.	Power domain	Type	Description	Note
STATUS	42	1.8V	DO	Module operation status indication	If unused, keep it open.

The recommended reference design is as follows:

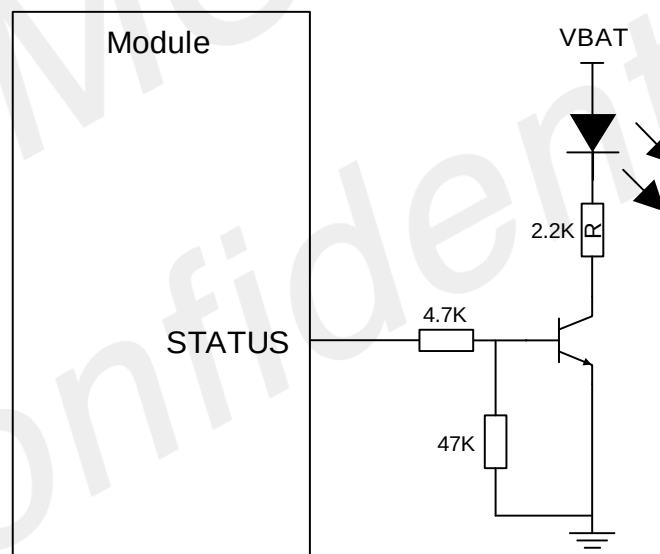


Figure 23: STATUS reference circuit

NOTE

The value of the resistor named “R” depends on the LED characteristic.

3.12. NETLIGHT Interface

NETLIGHT can indicate the current network status. It is usually used to drive the LED light indicating the network status.

Table 33: NETLIGHT interface pin definition

Pin name	No.	Power domain	Type	Description	Note
NETLIGHT	41	1.8V	DO	Network registration status indicator (LED).	

The recommended reference design is as follows:

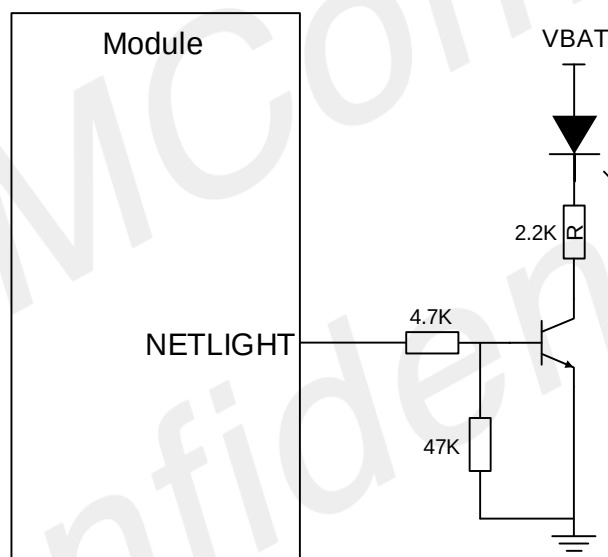


Figure 24: NETLIGHT reference circuit

NOTE

The value of the resistor named “R” depends on the LED characteristic.

The NETLIGHT signal is used to control the LED light that indicates the status of the network. The working status of this pin is shown in the table below.

Table 34: LTE mode NETLIGHT pin status

NETLIGHT pin status	Module status
Always On	Searching Network
200ms ON, 200ms OFF	Data Transmit/Registered
OFF	Power off / Sleep

3.13. Other Interface

3.13.1. ADC

The module has two general ADC pins. Built-in VBAT ADC interface.

Table 35: ADC interface pins definition

Pin name	No.	Power domain	Type	Description	Note
ADC1	38	0V-1.2V	AI	General Purpose ADC	If unused, keep it open.
ADC2	66	0V-1.2V	AI	General Purpose ADC	

The electrical characteristics are as follows:

Table 36: General ADC electronic characteristics

Characteristics	Min.	Typ.	Max.	Unit
Resolution	-	12	-	Bits
Input Range	0	-	1.2	V
Input Resistance		Hi-Z		

NOTE

1. "AT+CADC=2" can be used to read the voltage of the ADC1 pin.
2. "AT+CADC2=2" can be used to read the voltage of the ADC2 pin.
3. "AT+CBC" can be used to read the voltage of the VBAT.
4. For more details, please refer to document [1].

3.13.2. VDD_EXT

The module provides 1 LDO outputs: VDD_EXT.

VDD_EXT can only provide a current capacity of 50mA. It cannot be used as a high current drive source.

Table 37: VDD_EXT interface pin definition

Pin name	No.	Power domain	Type	Description	Note
VDD_EXT	40	-	PO	1.8V power output, output current up to 50 mA.	Default on. If unused, keep it open.

Table 38: VDD_EXT electrical characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD_EXT}	Output voltage	-	1.8	-	V
I_o	Output current	-	-	50	mA

The recommended reference design is as follows:

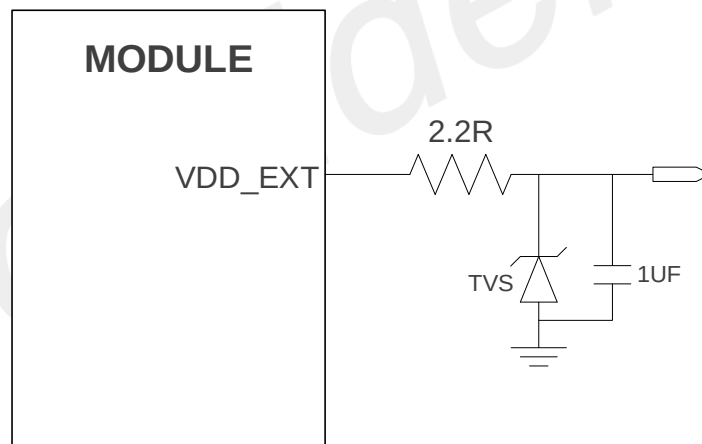


Figure 25: VDD_EXT reference circuit

NOTE

VDD_EXT is the module power supply. If the damage will affect the system startup, it is recommended that customers add TVS protection. The recommended model is ESD56051N.

Table 39: TVS for VDD_EXT part number list

Manufacturer	Part Number	V_{RWM}	$V_C(Max)$	$C_J(Max)$	Package
WILLSEMI	ESD56051N-2/TR	3.3V	10V	65F	DFN1006-2L

SIMCom
Confidential

4. RF Specifications

4.1. LTE Specifications

Table 40: Conducted transmission power

Frequency	Power	Min.
LTE-FDD B1	23dBm +/-2.7dB	<-40dBm
LTE-FDD B3	23dBm +/-2.7dB	<-40dBm
LTE-FDD B5	23dBm +/-2.7dB	<-40dBm
LTE-FDD B8	23dBm +/-2.7dB	<-40dBm
LTE-TDD B34	23dBm +/-2.7dB	<-40dBm
LTE-TDD B38	23dBm +/-2.7dB	<-40dBm
LTE-TDD B39	23dBm +/-2.7dB	<-40dBm
LTE-TDD B40	23dBm +/-2.7dB	<-40dBm
LTE-TDD B41	23dBm +/-2.7dB	<-40dBm

Table 41: E-UTRA operating bands

E-UTRA	UL Freq.	DL Freq.	Duplex Mode
1	1920~1980 MHz	2110~2170 MHz	FDD
3	1710~1785 MHz	1805~1880 MHz	FDD
5	824~849 MHz	869~894MHz	FDD
8	880~915 MHz	925~960 MHz	FDD
34	2010~2025 MHz	2010~2025 MHz	TDD
38	2570 ~2620 MHz	2570 ~2620 MHz	TDD
39	1880 ~1920 MHz	1880 ~1920 MHz	TDD
40	2300 ~2400 MHz	2300 ~2400 MHz	TDD
41	2535 ~2655 MHz	2535 ~2655 MHz	TDD

Table 42: Conducted receive sensitivity

Frequency	Receive sensitivity(Typical)	Receive sensitivity(MAX)
LTE FDD/TDD	Refer to the table 43	3GPP

Table 43: Reference sensitivity (QPSK)

E-UTRA Band	3GPP TS36.521-1						Actual 10 MHz	Duplex Mode
	1.4 MHz	3MHz	5MHz	10MHz	15 MHz	20 MHz		
1	-	-	-99.3	-96.3	-94.5	-99	-99.5	FDD
3	-101	-98	-96.3	-91.5	-90.3	-97	-99	FDD
5	-102	-99	-97.3	-94.3	-	-	-96.5	FDD
8	-102.2	-99.2	-97	-94	-	-	-100	FDD
34	-	-	-100	-97	-95.2	-	-101.5	TDD
38	-	-	-100	-97	-95.2	-94	-101.5	TDD
39	-	-	-100	-97	-95.2	-94	-101.5	TDD
40	-	-	-100	-97	-95.2	-94	-101.5	TDD
41	-	-	-99	-96	-94.2	-93	-101	TDD

4.2. LTE Antenna Requirements

For better overall performance, it is recommended that the antenna design should refer to the index requirements in the following table.

Table 44: LTE antenna requirements

Passive	Recommended standard
Operating band	Please refer to the table 42 and table 43
Direction	Omnidirectional
Gain	> -3dBi (Avg)
Input impedance	50 ohm
Efficiency	> 50 %
Maximum input power	50W
VSWR	< 2
Isolation	>20dB
PCB insertion loss(<1GHz)	<0.5dB
PCB insertion loss(1GHz~2.2GHz)	<1dB
PCB insertion loss(2.3GHz~2.7GHz)	<1.5dB

4.3. Antenna Reference Design

4.3.1. Passive Antenna for LTE/GNSS

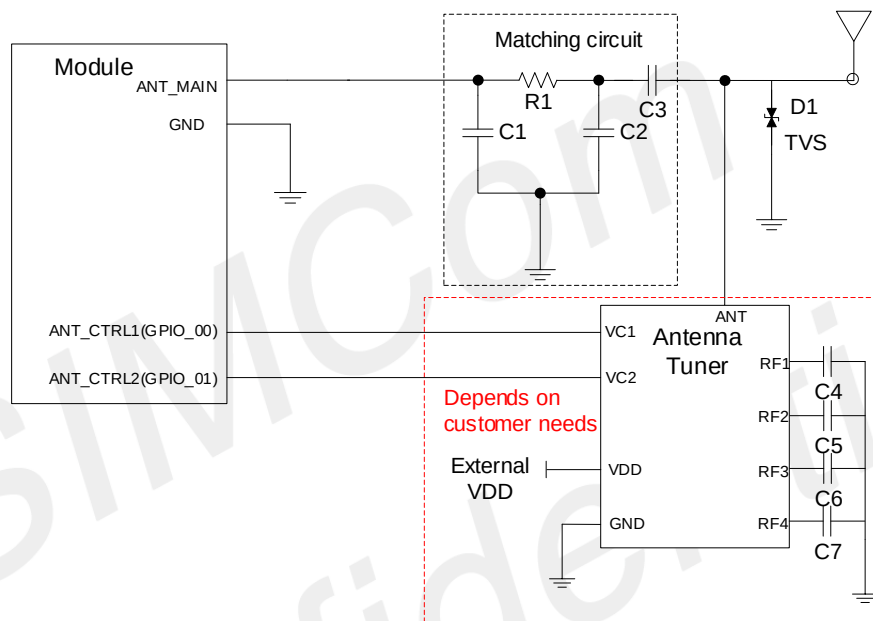


Figure 26: Passive antenna reference

The matching circuit R1 is labeled 0Ω by default, and C1 and C2 are reserved by default, and the specific value is determined by the antenna optimization, usually provided by the antenna manufacturer.

The Pins 78 and 79 are reserved for the LTE Antenna tuner, which is dependent on the specific requirements of the customer. If there is a need to use the antenna tuner, please refer to the design document "Antenna Tuning Reference Design" for design details.

The antenna port is easy to introduce static electricity, to avoid the internal components of the module being damaged by static electricity, C3 is pasted with a 100pF capacitor by default to enhance ESD protection capability.

It is recommended that D1 choose a suitable two-way TVS protection device placed close to the antenna. It especially needs to pay attention to the influence of TVS junction capacitance value on RF signals. Recommended TVS models are as follows:

Table 45: TVS for RF main antenna part number list

Manufacturer	Part Number	V_{RWM}	$V_C(\text{Max})$	$C_J(\text{Max})$	Package
INPAQ	CES10201V05B0	5V	30V	0.1pF	0201
BiILSEMI	BLE5V0CR05UB	5V	40V	0.05pF	DFN1006-2L

Table 46: TVS for GNSS antenna part number list

No.	manufac turer	Part number	V_{RWM}	$V_C(\text{max})$	PPP(max)	$C_J(\text{Max.})$	Package
1	WAYON	WE05DGCF-B	5V	23V	70W	0.3pF	DFN1006-2

4.3.2. Active Antenna for GNSS

The GNSS active antenna reference circuit is shown below:

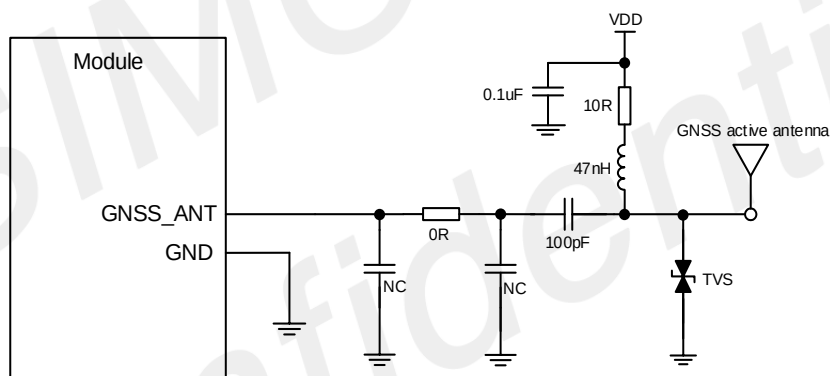


Figure 27: Active antenna reference

※ Note

1. GNSS adopts the active antenna design scheme by default, and C uses 100pF by default. For customers using the passive antenna scheme, it is recommended to disconnect the power supply path to avoid chip damage caused by passive antenna installation.
2. There may be parallel inductance at the antenna inside the module, showing a similar short circuit phenomenon, which is normal. Please consult SIMCom if you have any doubts about this.

5. Electrical Specifications

5.1. Absolute maximum ratings

Absolute maximum rating for digital and analog pins of A7682S R5 are listed in the following table, exceeding these limits may cause permanent damage to the module.

Table 47: Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage on VBAT	-0.5	-	4.8	V
Voltage on USB_VBUS	-0.5	-	5.4	V
Voltage at digital pins (GPIO, I2C, UART, PCM)	-0.3	-	2.0	V
Voltage at I/O pins (USIM)	-0.3	-	2.0	V
	-0.3	-	3.9	V
Voltage at PWRKEY\RESET	-0.3	-	4.8	V

5.2. Operating conditions

Table 48: Recommended operating ratings

Parameter	Min.	Typ.	Max.	Unit
Voltage at VBAT	3.4	3.8	4.2	V
Voltage at USB_VBUS	3.0	5.0	5.2	V

Table 49: 1.8V Digital I/O characteristics*

Parameter	Description	Min.	Typ.	Max.	Unit
V _{IH}	High-level input voltage	VCC*0.7	1.8	VCC+0.2	V
V _{IL}	Low-level input voltage	-0.3	0	VCC*0.3	V
V _{OH}	High-level output voltage	VCC-0.2	-	-	V
V _{OL}	Low-level output voltage	0	-	0.2	V
I _{OH}	High-level output current (no pull	-	-	42	mA

	down resistor)				
I_{OL}	Low-level output current (no pull up resistor)	-	-	49	mA
I_{IH}	Input high leakage current (no pull-down resistor)	-	-	10	uA
I_{IL}	Input low leakage current (no pull up resistor)	-10	-	-	uA

NOTE

These parameters are for digital interface pins, such as GPIO, I2C and UART.

The operating temperature of A7682S R5 is listed in the following table.

Table 50: Operating temperature

Parameter	Min.	Typ.	Max.	Unit
Normal operation temperature	-30	25	75	°C
Extended operation temperature*	-40	-	85	°C
Storage temperature	-45	-	90	°C

NOTE

When Module is within the extended operation temperature range, Module is able to establish and maintain data transmission, SMS, etc. The performance may deviate slightly from the 3GPP specifications, but will meet 3GPP specifications again when the temperature returns to normal operating temperature levels. It is strongly recommended that customers take heat dissipation measures to ensure that the normal operating temperature of the module can't be exceeded.

5.3. Operating Mode

5.3.1. Operating Mode Definition

The table below summarizes the various operating modes of module.

Table 51: Operating mode Definition

Mode		Function
Normal operation	LTE Sleep	AT command “AT+CSCLK=1” can be used to set the module to sleep mode. In this case, the current consumption of module will be reduced to the minimal level and the module can still receive paging message and SMS.
	LTE Idle	Software is active. Module is registered to the network, and the module is ready to communicate.
	LTE Talk	Two customers are connected. In this case, the power consumption of the module depends on the network and module configuration.
	LTE Data transmission	There is data transmission in progress. In this case, power consumption is related to network settings (e.g., power control level); uplink/downlink data rates, etc.
Minimum functionality mode		AT command ‘AT+CFUN=0’ can be used to set the module to a minimum functionality mode without removing the power supply. In this mode, the RF part of the module will not work and the USIM card will not be accessible, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
Flight mode		AT command ‘AT+CFUN=4’ can be used to set the module to flight mode without removing the power supply. In this mode, the RF part of the module will not work, but the serial port and USB port are still accessible. The power consumption in this mode is lower than normal mode.
PSM mode		The module can be set to PSM mode by AT command without removing the power supply. In this mode, the CPU is powered off, only the clock circuit inside the module works, the network is not connected, and the serial port and USB are unavailable. In this case, the power consumption of the module is reduced to the minimum.
Power off		Module will go into power off mode by sending the AT command ‘AT+CPOF’ or pull down the PWRKEY pin, normally. In this mode the power management unit shuts down the power supply, and software is not active. The serial port and USB are not accessible.

5.3.2. Sleep mode

In sleep mode, the current consumption of module will be reduced to the minimal level, and module can still receive paging message and SMS.

Both hardware and software should meet several conditions simultaneously so that A7682S R5 will enter into sleep mode:

- USB condition: Send 'AT+CSCLK=1' and unplug USB.
- Software condition: Software must support sleep mode configuration.
- UART condition: Send 'AT+CSCLK=1'.

NOTE

Before designing, please pay attention to how to realize sleeping/waking function and refer to document [17] for more details.

5.3.3. Minimum functionality mode and Flight mode

Minimum power consumption mode ceases a majority function of Module, to enable the module enter the minimum power consumption mode, the following hardware and software conditions must be followed:

- (1) Module is in normal mode.
- (2) Send AT command "AT+CFUN=0".
- (3) Send AT command "AT+CSCLK=1".
- (4) DTR pin pulled to high level and USB_VBUS pulled to low level.

This mode is set by the AT command which provides a choice of the functionality levels.

- AT+CFUN=0: Minimum functionality
- AT+CFUN=1: Full functionality (Default)
- AT+CFUN=4: Flight mode

If A7682S R5 has been set to minimum functionality mode, the RF function and SIM card function will be closed. In this case, the serial port and USB are still accessible, but RF function and SIM card will be unavailable.

If A7682S R5 has been set to flight mode, the RF function will be closed. In this case, the serial port and USB are still accessible, but RF function will be unavailable.

When A7682S R5 is in minimum functionality or flight mode, it can return to full functionality by the AT command "AT+CFUN=1".

5.3.4. PSM mode

The PSM mode can be set by “AT+CPSMS”, and it can minimize the current consumption.

The module is initially in the RRC connect state, and it will enter idle mode after disconnecting RRC Connect by “end call”, while the timer T3324/T3412 starts timing. After the timer T3324 expires, the module enters the PSM mode. The module will wake up automatically after the timer T3412 expiring, and it will enter TAU mode.

The AT command for entering the PSM mode are as follows:

AT*COMCFG=1,,,,,254//Enable the 1bis

AT+CFUN=0

AT+CPSMS=1,,,"01100101","00000101"//Open the PSM

AT+MEDCR=0,103,1

AT+MEDCR=0,71,2//Set the wake-up time to 2 minutes

AT+CFUN=1

After entering the PSM mode, the module will terminate the network connection, and unable to respond to requests. Customers can send AT command when the timer T3412 expiring or pull down the PWRKEY to wake up the module. The module will exit the PSM mode by “AT+CPSMS=0”.

5.4. Current Consumption

5.4.1. Current Consumption of VBAT

The current consumption is listed in the table below.

Table 52: Current consumption on VBAT Pins (VBAT=3.8V)

PSM mode	
PSM supply current	Typical: 8uA
LTE sleep/Idle mode	
LTE supply current (Without USB connection)	Idle mode Typical: 8mA Sleep mode@DRX=0.32S typical: 1.22mA Sleep mode@DRX=0.64S typical: 0.92mA Sleep mode@DRX=1.28S typical: 0.72mA Sleep mode@DRX=2.56S typical: 0.61mA
Minimum functionality mode	
AT+CFUN=0, AT+CSCLK=1	Typical: 482uA (With simcard) Typical: 542uA (Without simcard)
LTE Cat1	
LTE-FDD B1	@10MHz 23dBm Typical :542mA

LTE-FDD B3	@10MHz	23dBm	Typical :630mA
LTE-FDD B5	@10MHz	23dBm	Typical :626mA
LTE-FDD B8	@10MHz	23dBm	Typical :587mA
LTE-TDD B34	@10MHz	23dBm	Typical :546mA
LTE-TDD B38	@10MHz	23dBm	Typical :487mA
LTE-TDD B39	@10MHz	23dBm	Typical :566mA
LTE-TDD B40	@10MHz	23dBm	Typical :608mA
LTE-TDD B41	@10MHz	23dBm	Typical :554mA

5.4.2. Current Consumption of GNSS

Table 53: Current consumption on VBAT Pins (VBAT=3.8V)
(VBAT=3.8V, @AT+CFUN=0, AT+CSCLK=1, without USB connection)

Mode	Positioning system	Condition	Typical value (mA)
GNSS signal generator	GPS	-130dBm/Tracking	26.65
		-145dBm/Tracking	27.08
		-130dBm/ Cold start	26.25
		-145dBm/ Cold start	26.04
	GPS+BD	-130dBm/Tracking	27.05
		-145dBm/Tracking	27.50
		-130dBm/ Cold start	27.43
		-145dBm/ Cold start	26.21
	GPS+GLONASS+BD	-130dBm/Tracking	27.98
		-145dBm/Tracking	28.07
		-130dBm/ Cold start	28.05
		-145dBm/ Cold start	26.68
Real network passive antenna	GPS	Acquisition	26.75
		Tracking	26.43
	GPS+BD	Acquisition	28.41
		Tracking	27.83
	GPS+GLONASS+BD	Acquisition	29.10
		Tracking	28.36

5.5. ESD Notes

A7682S R5 is sensitive to ESD in the process of storage, transporting, and assembling. When A7682S R5 is mounted on the customers' mother board, the ESD components should be placed beside the connectors which human body may touch, such as SIM card holder, audio jacks, switches, keys, etc. The following table shows the A7682S R5 ESD measurement performance.

Table 54: The ESD performance measurement table (Temperature: 25℃, Humidity: 45%)

Part	Contact discharge	Air discharge
VBAT, GND	±4V	±8V
Antenna port	±4V	±8V
USB interface	±4V	±6V
UART interface	±3V	±6V
USIM interface	±3V	±6V
Other PADS	±1V	±2V

NOTE

Test conditions:

- The external of the module has surge protection diodes and ESD protection diodes.
- The data in table above were tested using SIMCom EVB.

6. SMT Production Guide

6.1. Top and Bottom View of the module

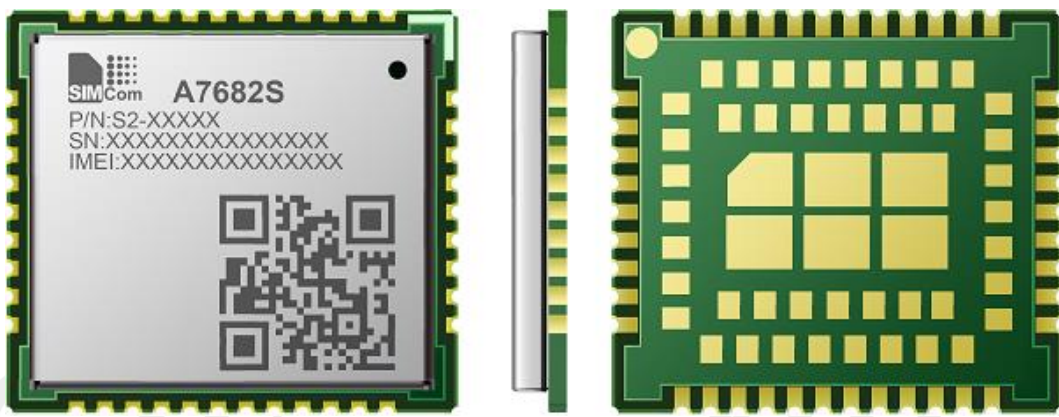


Figure 29: Top and bottom view of the module

NOTE

The above is the design effect diagram of the module for reference. The actual appearance is subject to the actual product.

6.2. Label Information

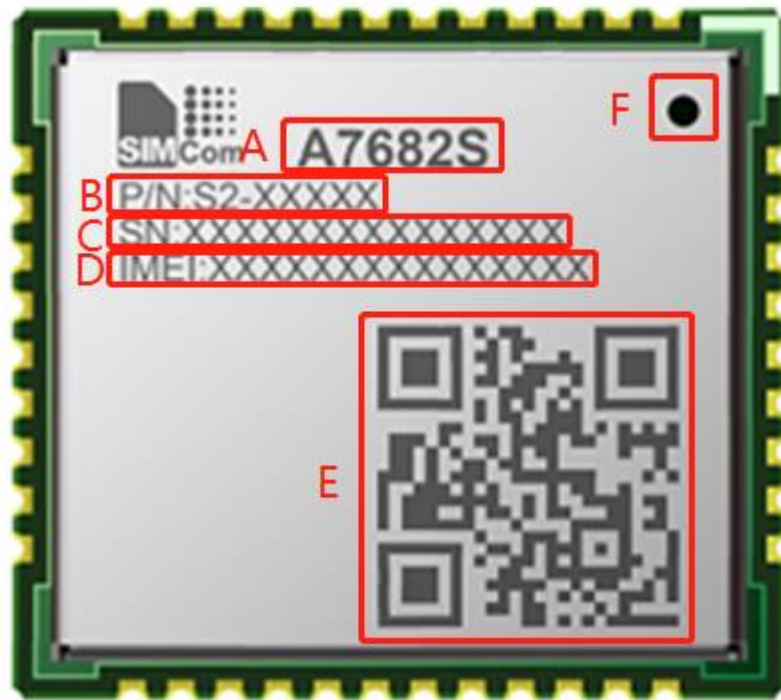


Figure 30: Label description of the module

Table 55: The description of label information

No.	Description
A	Project name
B	Product number
C	Serial number
D	IMEI number
E	QR code
F	Module 1 pin identification

6.5. Recommended reflow furnace temperature curve

It is recommended to lead free.

During the furnace temperature test, the thermocouple test point should be connected to the module position to ensure that the module position reaches the required temperature. Recommended furnace temperature profile (lead-free SMT reflow) is as follows:

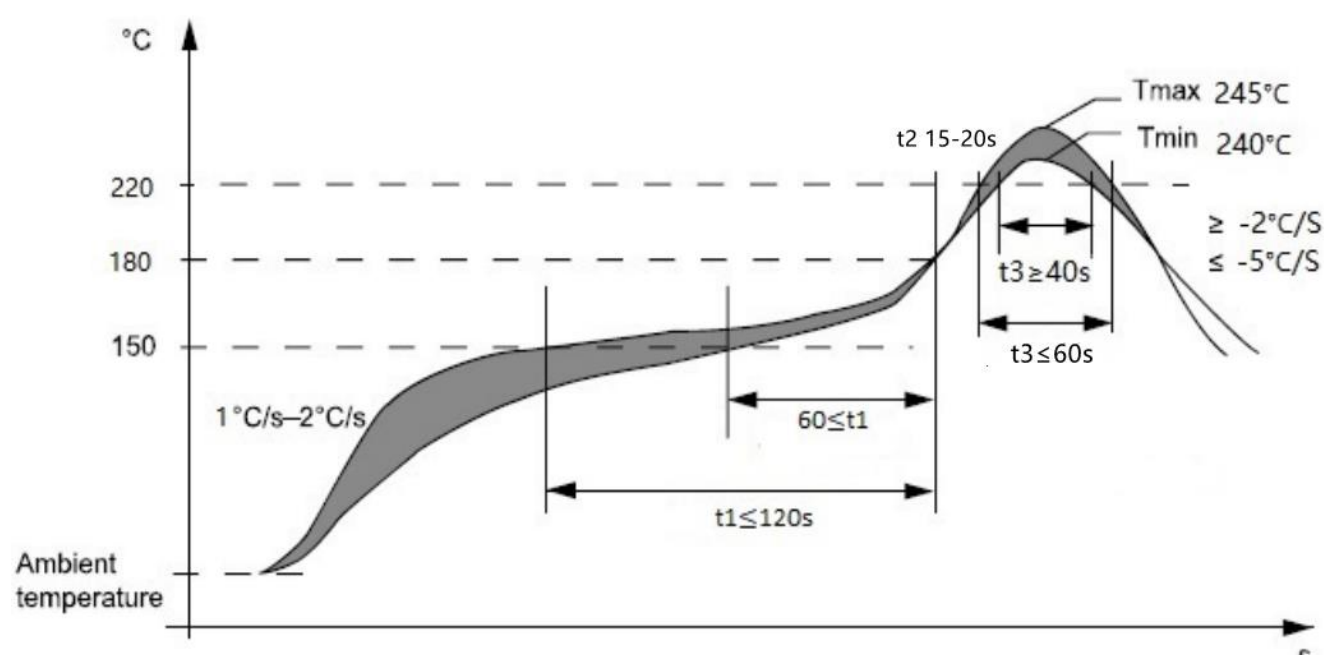


Figure 33: Recommended reflow furnace temperature curve (lead-free)

Table 56: The main board reflux temperature curve requirements (lead-free)

Temperature range	Time	Critical parameter
Preheating zone (Room temperature~150 °C)	NA	Temperature rise slope 1~2°C/s
T1(150~180°C)	60-120s	/
T2(180-220°C)	15-20s	/
T3(≥220°C)	40-60s	Peak temperature 240~245°C
Cooling Zone	NA	Cooling slope -2~-5°C/s

NOTE

- The maximum times of refluxes for the module is once.
- Recommended lead-free process.
- In the table above, the temperature testing location includes the solder mask of the module MCU pins, bottom LGA pins, and external LCC pins.
- The actual welding temperature is affected by other external factors, such as the presence of furnace carriers, solder paste, size and thickness of the substrate, and component resistance. Thermal requirements and panel design, etc. Please confirm with our engineering and technical personnel in time if the recommended parameters cannot be reached. Otherwise, the module may be damaged.
- For boards with thickness less than 1.2mm, it is recommended to use board supported by furnace carrier or materials with high Tg to prevent warping when heated. Deformation, thus affecting module welding. For modules larger than 35.0 mm *35.0 mm and 5G products, it is recommended to use the furnace carrier to pass through the furnace to reduce the cause of the bottom plate and mold. Due to the difference of Tg value of block, the phenomenon of unbalanced thermal stress appears in the process of high temperature welding reflow, resulting in the defect rate of virtual welding and little tin.
- After the module is welded, X-ray and optical inspection methods shall be used to check the welding quality. For specific standards, please refer to relevant standards of IPC-A-610H.
- For more information about shipping and manufacturing, please refer to [Module Secondary SMT Process User Guide](#).
- Due to the complexity of the SMT process, in case of uncertainty or processes not mentioned in this document (such as selective wave soldering, ultrasonic welding), please contact SIMCom support team before SMT process starts.

6.6. Moisture Sensitivity Level (MSL)

The modules are shipped in vacuum-sealed aluminum foil bag bags, vacuum packaging according to IPC/JEDEC standard J-STD-020C specification.

- Recommended storage conditions: temperature $23^{\circ}\text{C} \pm 5^{\circ}\text{C}$, and relative humidity 35%~60%.
- Storage period: 12 months (Under recommended storage conditions and in sealed vacuum packaging).

The module meets the humidity sensitivity level 3 (MSL-3), and the storage period after unpacking is shown in table below.

The out-of-bag floor life of the module with MSL-3 is 168 hours. If the workshop temperature is $23^{\circ}\text{C} \pm 5^{\circ}\text{C}$ and the relative humidity is less than 60%, the module needs to be unpacked within 168 hours of reflux production or other high temperature operations. Otherwise, the module shall be stored in an environment with relative humidity less than 10% (for example, a moisture-proof cabinet) to keep the product dry.

Table 57: Moisture Sensitivity Level

MSL	Out-of-bag floor life	Comment
1	Unlimited	≤+30℃/85% RH
2	1 year	≤+30℃/60% RH
2a	4 weeks	
3	168 hours	
4	72 hours	
5	48 hours	
5a	24 hours	
6	Mandatory bake before use. After bake, it must be reflowed within the time limit specified on the label.	

Before using, it is necessary to confirm whether the package is in good condition. After unpacking, check the status of humidity indicator card in vacuum bag (Figure 34). The module needs to be baked before use if any of the following conditions occur.

- Explanation Humidity indicator card: 30%, 40%, and 50% of any indicator circle has discolouring.
- The module has been un-packed and the module exceeds the humidity sensitivity level corresponding to the exposed workshop time. For example, MSL=3 is 168.
- Packed, but the Shelf Life exceeds 12 months.
- Exceeds the Floor Life.
- Unable to track and determine the status of the module.

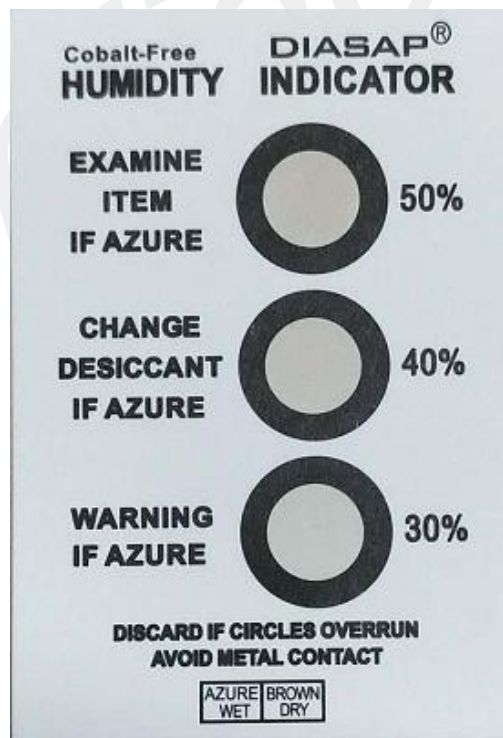


Figure 34: Humidity card

The following conditions also need to be pre-baked.

- The storage temperature and humidity do not meet the recommended storage conditions.
- Vacuum sealed bag leak, bulk materials.
- Before repairing the module.
- After unpacking, the module failed to complete production or storage under the control of humidity sensitive level 3.

6.7. Baking Requirements

If baking is required, proceed according to the requirements in the table below. Preferentially choose a nitrogen-filled oven.

Table 58: Module baking requirements

Baking conditions	Baking time	Comment
120℃ ± 5℃, <5% RH	8 hours	Not applicable to original packaging pallets

NOTE

- In order to prevent and reduce the occurrence of poor welding caused by moisture, such as foaming and delamination, the module should be strictly controlled. It is not recommended to expose the module to air for a long time after unpacking the vacuum package.
- Before baking, it is necessary to remove the module from the package and place the bare module on the high temperature resistant device to avoid high temperature damage to the plastic tray or coil. The modules for secondary baking must be welded within 24 hours after baking. Otherwise, they need to be stored in vacuum packaging or in a drying oven.
- Please pay attention to ESD protection when unpacking and placing modules, such as wearing anti-static gloves.

7. Packaging

A7682S R5 module support tray packaging.

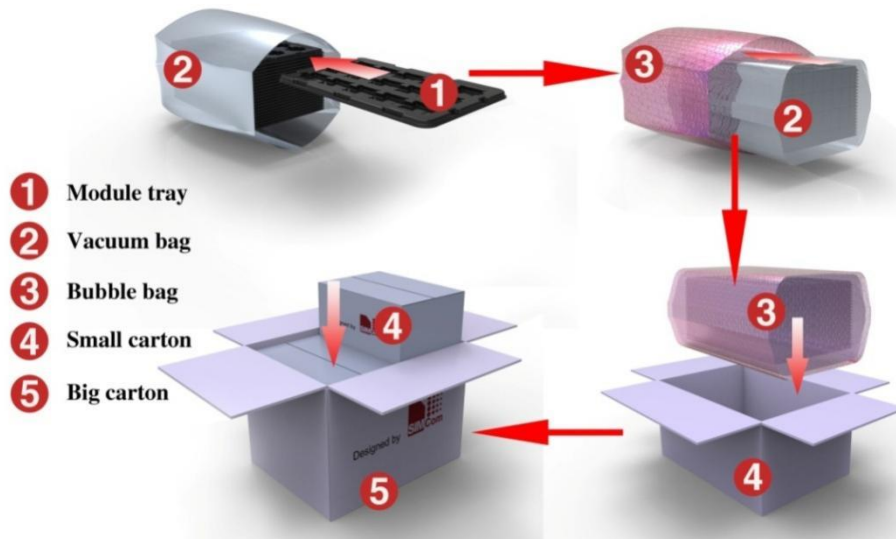


Figure 35: Packaging diagram

Module tray drawing:

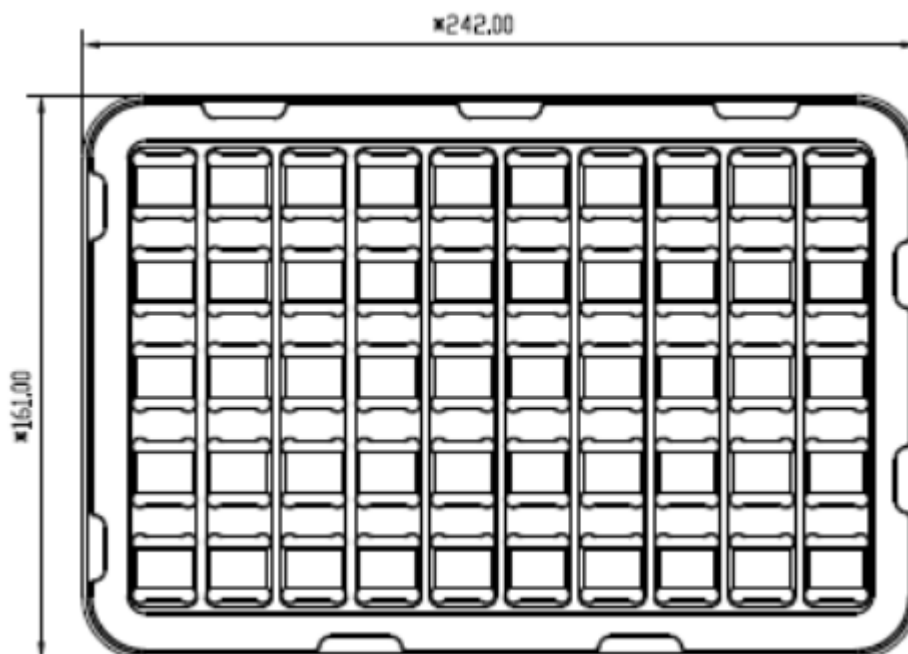


Figure 36: Tray drawing

Table 59: Tray size

Length ($\pm 3\text{mm}$)	Width ($\pm 3\text{mm}$)	Module number
242.0	161.0	50

Small carton drawing:

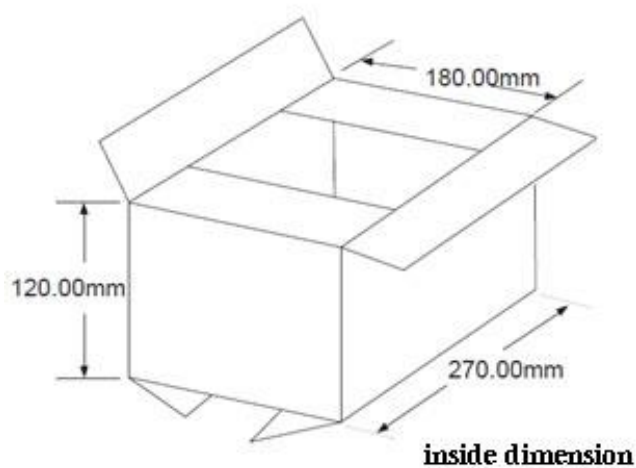


Figure 37: Small carton drawing

Table 60: Small Carton size

Length ($\pm 10\text{mm}$)	Width ($\pm 10\text{mm}$)	Height ($\pm 10\text{mm}$)	Module number
270	180	120	50*20=1000

Big carton drawing:

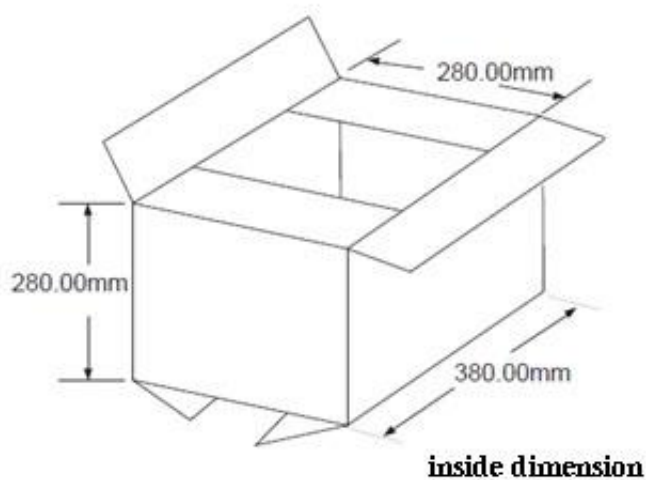


Figure 38: Big carton drawing

Table 61: Big Carton size

Length ($\pm 10\text{mm}$)	Width ($\pm 10\text{mm}$)	Height ($\pm 10\text{mm}$)	Module number
380	280	280	1000*4=4000

SIMCom
Confidential

8. Appendix

8.1. Coding Schemes and Maximum Net Data Rates over Air Interface

Table 62: Coding Schemes and Maximum Net Data Rates over Air Interface

LTE-FDD device category (Downlink)	Max data rate (peak)	Modulation type
Category 1	10Mbps	QPSK/16QAM/64QAM
LTE-FDD device category (Uplink)	Max data rate (peak)	Modulation type
Category 1	5Mbps	QPSK/16QAM

8.2. Related Documents

Table 63: Related Documents

NO.	Title	Description
[1]	A1602 & 1606_Series_AT_Command Manual_V1.03	AT Command Manual
[2]	ITU-T Draft new recommendation V.25ter	Serial asynchronous automatic dialing and control
[3]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[4]	3GPP TS 34.124	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[5]	3GPP TS 34.121	Electromagnetic Compatibility (EMC) for mobile terminals and ancillary equipment.
[6]	3GPP TS 34.123-1	Technical Specification Group Radio Access Network; Terminal conformance specification; Radio transmission and reception (FDD)

[7]	3GPP TS 34.123-3	User Equipment (UE) conformance specification; Part 3: Abstract Test Suites.
[8]	EN 301 908-02 V2.2.1	Electromagnetic compatibility and Radio spectrum Matters (ERM); Base Stations (BS) and User Equipment (UE) for IMT-2000. Third Generation cellular networks; Part 2: Harmonized EN for IMT-2000, CDMA Direct Spread (UTRA FDD) (UE) covering essential requirements of article 3.2 of the R&TTE Directive
[9]	EN 301 489-24 V1.2.1	Electromagnetic compatibility and Radio Spectrum Matters (ERM); Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment.
[10]	IEC/EN60950-1(2001)	Safety of information technology equipment (2000)
[11]	3GPP TS 51.010-1	Digital cellular telecommunications system (Release 5); Mobile Station (MS) conformance specification
[12]	GCF-CC V3.23.1	Global Certification Forum - Certification Criteria
[13]	2002/95/EC	Directive of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)
[14]	Module Secondary SMT Process User Guide_V1.xx	Module secondary SMT Guidelines
[15]	A76XX Series_UART_Application Note_V1.00	This document describes how to use UART interface of SIMCom modules.
[16]	Antenna design guidelines for diversity receiver system	Antenna design guidelines for diversity receiver system
[17]	A76XX Series_Sleep Mode_Application Note_V1.00	Sleep Mode Application Note
[18]	A76XX Series_UIM HOT SWAP_Application Note_V1.00	This document introduces UIM card detection and UIM hot swap.

8.3. Terms and Abbreviations

Table 64: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
ARP	Antenna Reference Point
BER	Bit Error Rate
BD	BeiDou
BTS	Base Transceiver Station
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processor
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
DAM	Downloadable Application Module
DPO	Dynamic Power Optimization
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FCC	Federal Communications Commission (U.S.)
FD	SIM fix dialing phonebook
FDMA	Frequency Division Multiple Access
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global Standard for Mobile Communications
HR	Half Rate
I2C	Inter-Integrated Circuit
IMEI	International Mobile Equipment Identity

LTE	Long Term Evolution
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
NMEA	National Marine Electronics Association
PAP	Password Authentication Protocol
PBCCH	Packet Switched Broadcast Control Channel
PCB	Printed Circuit Board
PCS	Personal Communication System, also referred to as GSM 1900
RF	Radio Frequency
RMS	Root Mean Square (value)
RTC	Real Time Clock
SIM	Subscriber Identification Module
SMS	Short Message Service
SMPS	Switched-mode power supply
TDMA	Time Division Multiple Access
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
VSWR	Voltage Standing Wave Ratio
EDGE	Enhanced data rates for GSM evolution
ZIF	Zero intermediate frequency
WCDMA	Wideband Code Division Multiple Access
VCTCXO	Voltage control temperature-compensated crystal oscillator
SIM	Universal subscriber identity module
UMTS	Universal mobile telecommunications system
UART	Universal asynchronous receiver transmitter
PSM	Power saving mode
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook
NC	Not connect

8.4. Safety Caution

Table 65: Safety Caution

Marks	Requirements
	When in a hospital or other health care facility, observe the restrictions about the use of mobiles. Switch the cellular terminal or mobile off, medical equipment may be sensitive and not operate normally due to RF energy interference.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. Forgetting to think much of these instructions may impact the flight safety, or offend local legal action, or both.
	Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard.
	Your cellular terminal or mobile receives and transmits radio frequency energy while switched on. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	Road safety comes first! Do not use a hand-held cellular terminal or mobile when driving a vehicle, unless it is securely mounted in a holder for hands free operation. Before making a call with a hand-held terminal or mobile, park the vehicle.
	GSM cellular terminals or mobiles operating over radio frequency signals and cellular networks cannot be guaranteed to connect in all conditions, especially with a mobile fee or an invalid SIM card. While you are in this condition and need emergent help, please remember to use emergency calls. In order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength. Some networks do not allow for emergency call if certain network services or phone features are in use (e.g. lock functions, fixed dialing etc.). You may have to deactivate those features before you can make an emergency call. Also, some networks require that a valid SIM card be properly inserted in the cellular terminal or mobile.